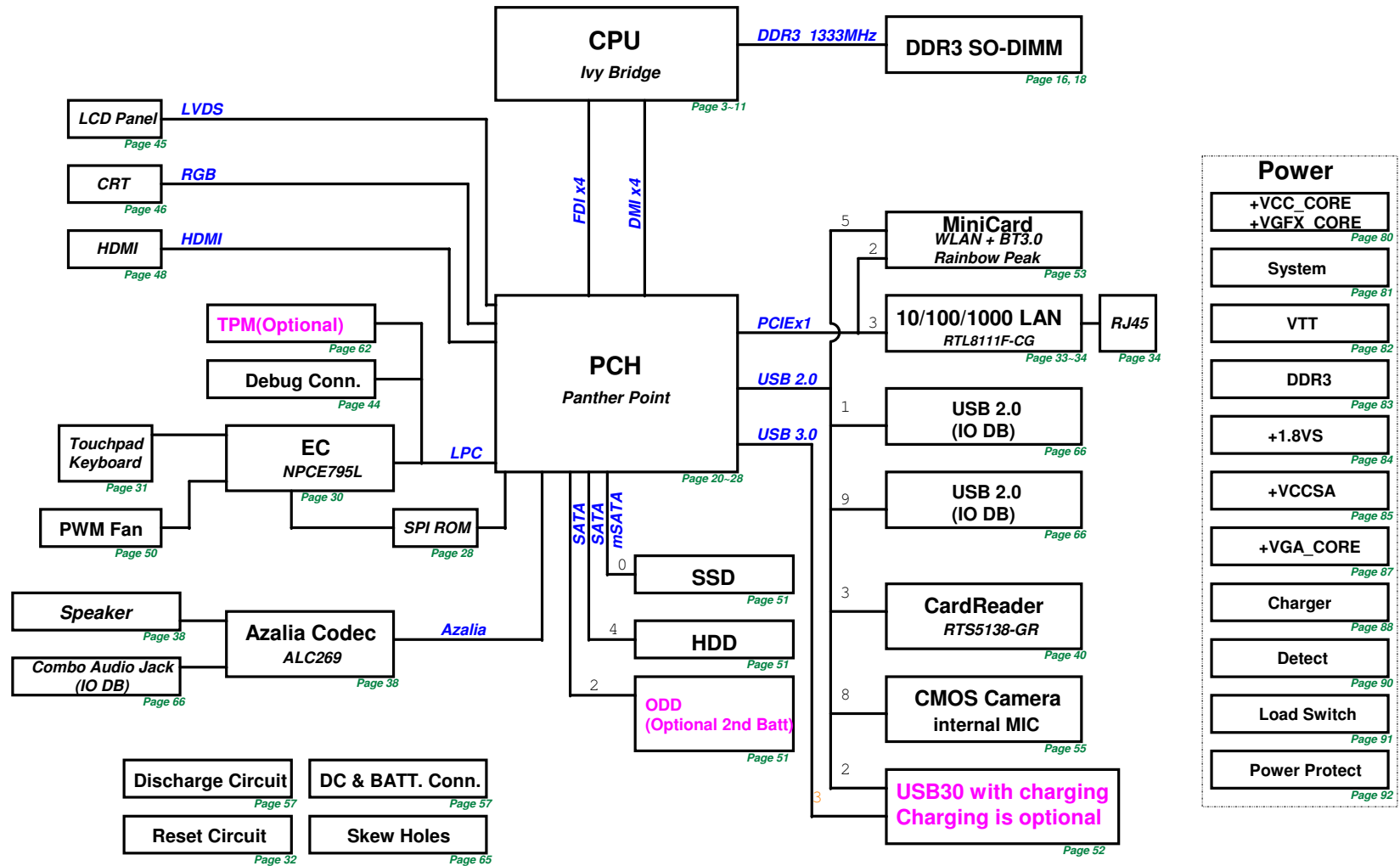


01. Block Diagram
02. System Setting
03. CPU(1)_DMI, DP, PEG, FDI
04. CPU(2)_CLK, MSIC, JTAG
05. CPU(3)_DDR3
06. CPU(4)_PROCSSOE POWER
07. CPU(5)_GRAPHIC POWER
08. CPU(6)_GND
09. CPU(7)_RESERVED
10. CPU_PCH_XDP
11. CPU DECOUPLING
16. DDR3(1)_SO-DIMM0
18. DDR3(3)_CA/DQ Voltage
20. PCH(1)_SATA, IHDA, RTC, LPC
21. PCH(2)_PCIE, CLK, SMB, PEG
22. PCH(3)_FDI, DMI, SYS PWR
23. PCH(4)_DP, LVDS, CRT
24. PCH(5)_PCI, NVRAM, USB
25. PCH(6)_CPU, GPIO, MISC
26. PCH(7)_POWER, GND
27. PCH(8)_POWER, GND
28. PCH(9)_SPI, SMB
29. CLK_IC9LS3197
30. EC_NPCE795(1)
31. EC_NPCE795(2) KB, TP
32. RST_Reset Circuit
33. LAN_RTL8111E
34. LAN_RJ45
38. AUD(1)_ALC269
40. CB(1)_RTS5138
44. BUG_Debug
45. CRT(1)_LVDS
46. CRT(1)_CRT
48. TV(1)_HDMI
50. FAN_Fan
51. mSATA, HDD, ODD
52. USB30 Port
53. MINICARD_WLAN
55. Camera
56. LED_Indicator
57. DSG_Discharge
60. DC_DC/BAT CONN
65. ME_CONN, Skew Hole
69. G-SENSOR*****
80. POWER_VCORE&VGFX
81. POWER_SYSTEM
82. POWER_VCCP
83. POWER_DDR & VTT
84. POWER_+1.8VS
85. POWER_0.85VS
87. POWER_+VGA_CORE(DSC)
88. POWER_CHARGER(ISL88731)
90. POWER_DETECT
91. POWER_LOAD SWITCH
92. POWER_PROTECT
93. POWER_SIGNAL
94. POWER_FLOWCHART
95. POWER_HISTORY
97. SYSTEM_HISTORY
98. Power On Sequence
99. Power On Timing

B34Y Chief River Platform(TACOMA FALL2) Rev 1.2

BLOCK DIAGRAM



PCH_CPT
GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
GPIO 37				
GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
GPIO 46				
GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

EC
NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
GPG0		
GPG1		
GPG2		
GPG6		
GPH0		
GPH1		
GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

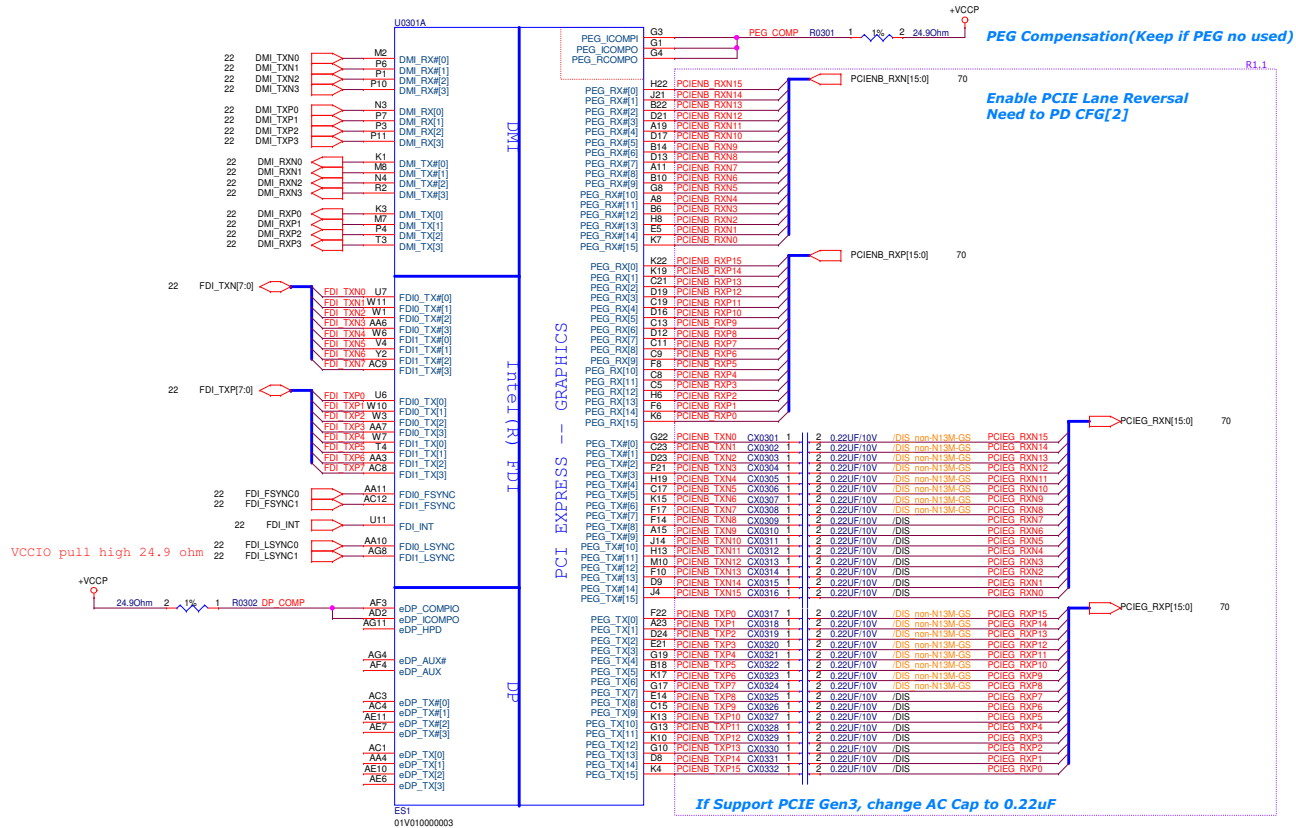
SM_BUS ADDRESS :

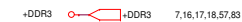
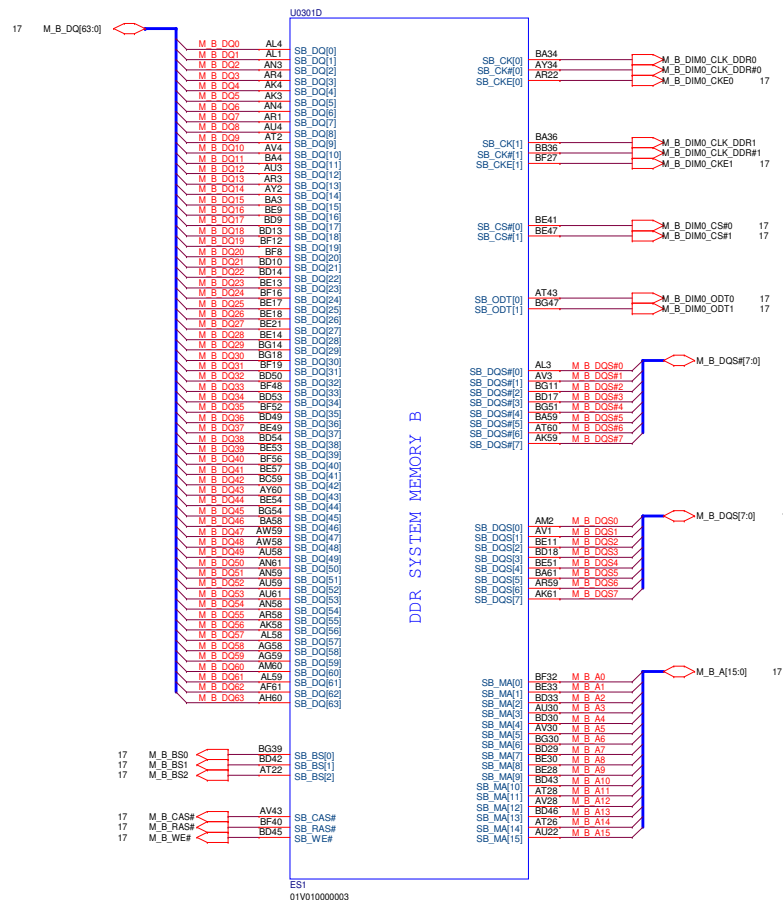
SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A







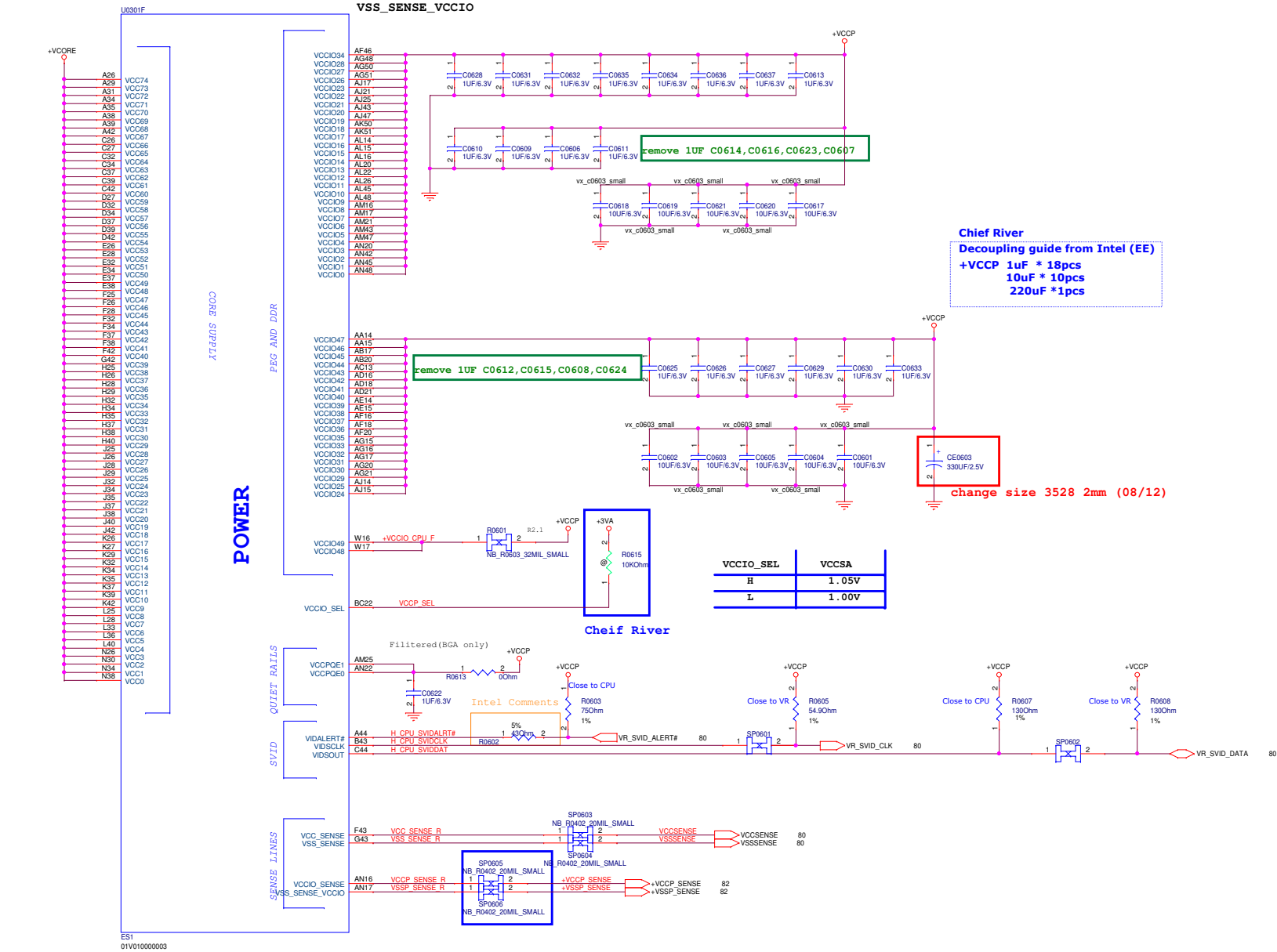
7,16,17,18,57,83

PEGATRON		Title :	CPU(3)_DDR3
BG1-1#W RD Div.2-#B RD Dept.5		Engineer:	Trunks Chen
Size C	Project Name B34	Rev 1.0	
Date: Wednesday, February 01, 2012		Sheet	5 of 59

Vcc for processor core
Voltage range: 0.3 - 1.52V

Voltage for the memory controller and
shared cache defined at the
motherboard VCCIO_SENSE and
VSS_SENSE_VCCIO

+VCCP  +VCCP 3,4,7,26,27,30,32,82
+VCCRE  +VCCRE 9,11,80



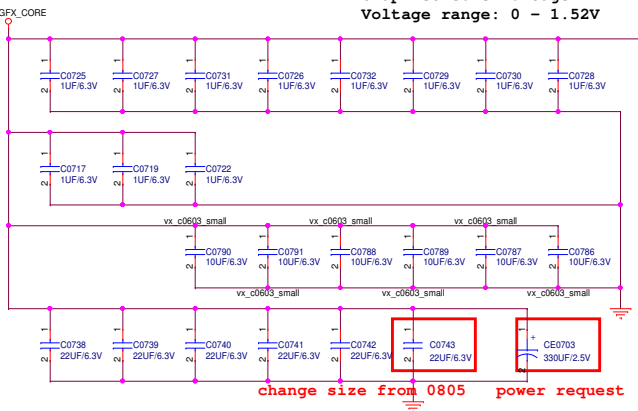
Chief River
Decoupling guide from Intel (EE)
+VCCP 1uF * 18pcs
10uF * 10pcs
220uF * 1pcs

change size 3528 2mm (08/12)

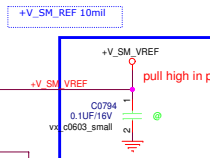
Chief River

Decoupling guide from Intel PDDG R0.8
+VGFX_CORE
 1uF * 11pcs
 10uF * 6pcs
 22uF * 6pcs

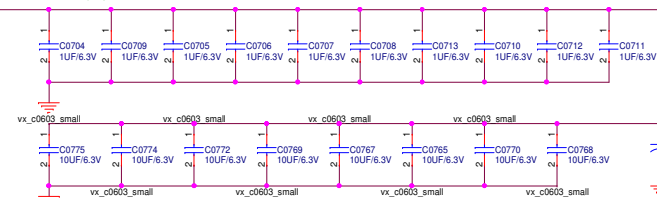
Graphics core voltage
Voltage range: 0 - 1.52V



change size from 0805 power request



MAX:10A



Processor I/O supply
voltage for DDR3
(DC + AC specification)

Chief River

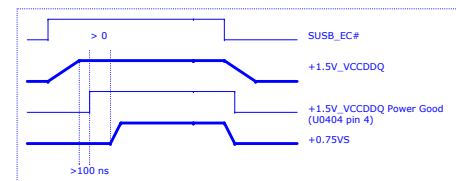
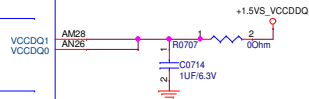
Decoupling guide from Intel (EE)

+1.5VS VCCDDO

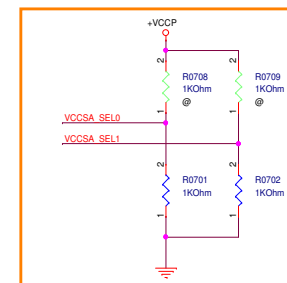
1uF * 10pcs

10uF * 8pcs

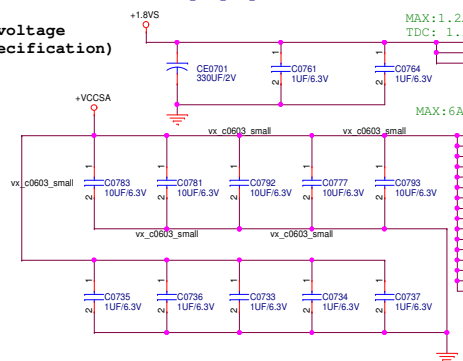
Filtered(BGA Only)



R1.0 0209
Intel Comments



PLL supply voltage
(DC + AC specification)



Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

GRAPHICS

1.8V RAIL LINES

SA RAIL

QUIZ RATLS

SENSE LINES

Chief River

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.725V
H	H	0.675V

PEGATRON Title : CPU(5) GFX PWR

BG1-HW RD Div.2-NB RD Dept.5		Engineer:	Trunks Chen
Size C	Project Name B34	Rev 1.0	
Date: Wednesday, February 01, 2012		Sheet	7 of 50

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition

- 0: Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort

- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6

- 10 : x 8 , x 8

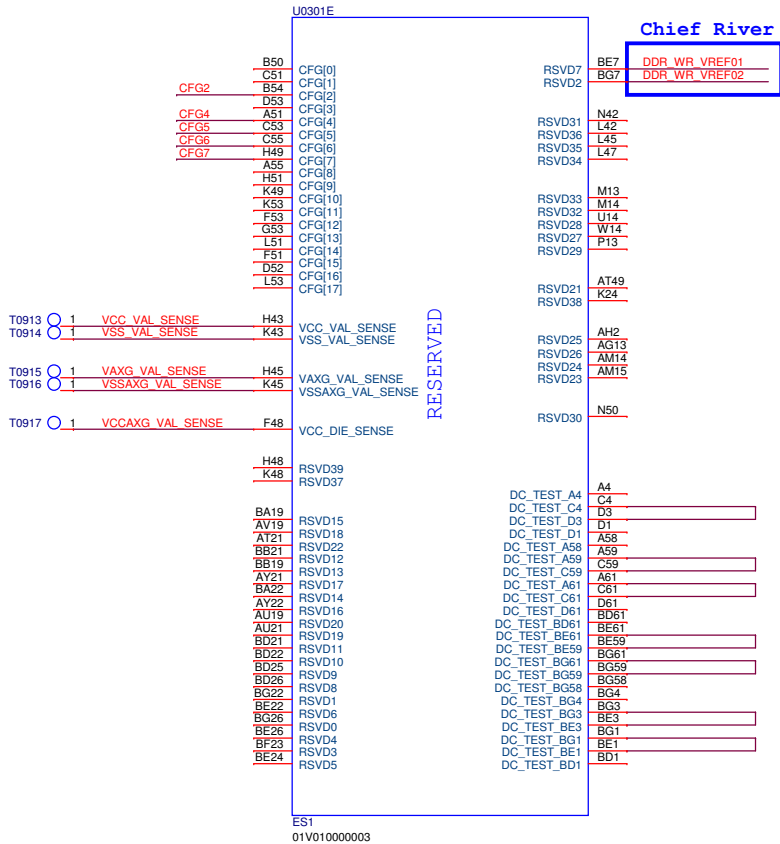
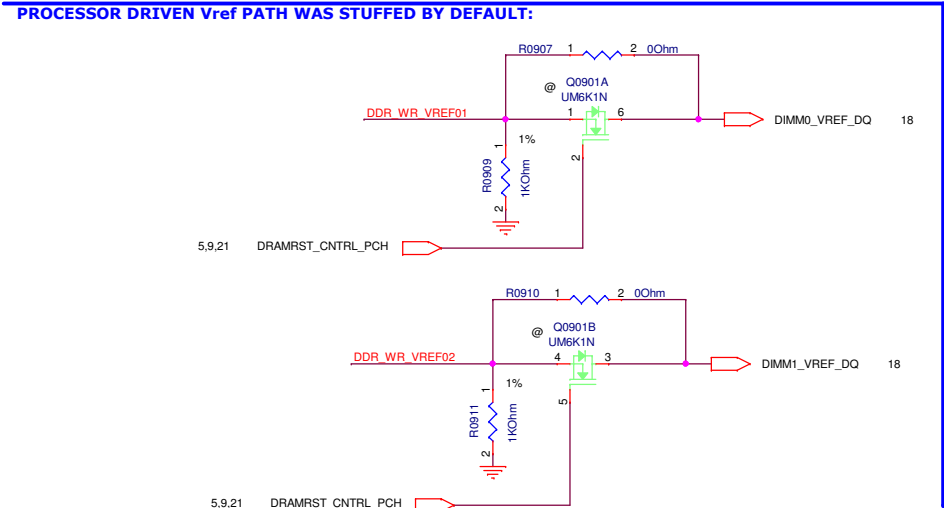
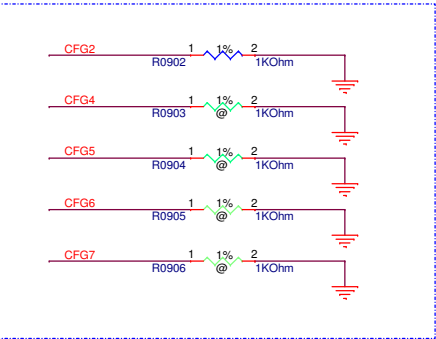
- 01 : Reserved

- 00 : x 8 , x 4 , x 4

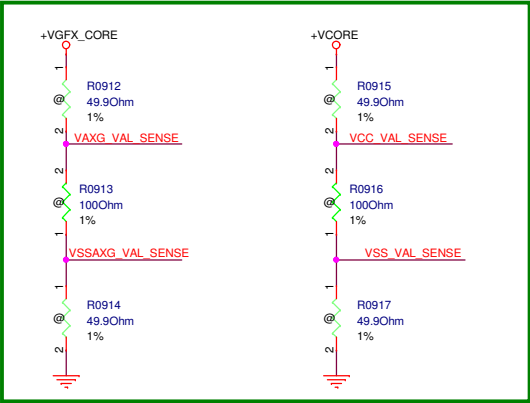
CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion

- 0: PEG Wait for BIOS training



For iFDIM testing
R0912~ R0917 close to pin < 1 inch



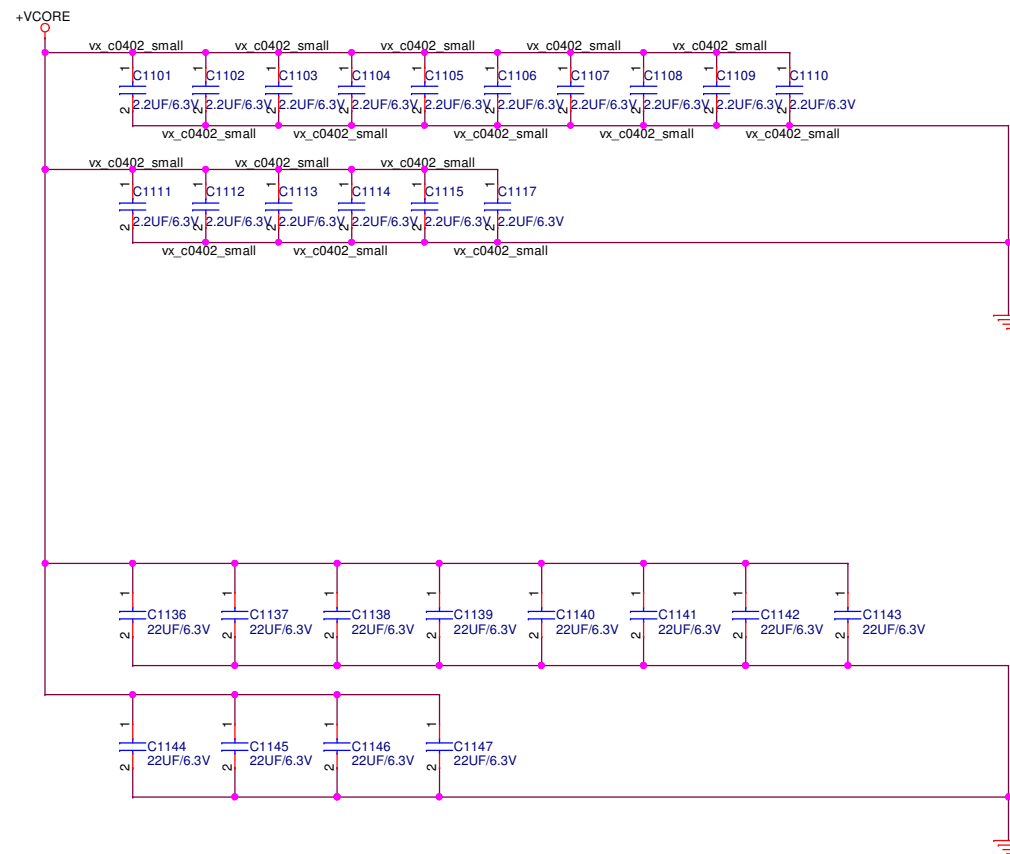


+VTT_PCH_ORG		+VTT_PCH_ORG	22,26,27
+3VSUS		+3VSUS	22,24,27,28,30,33,53,56,81,92
+VCCP		+VCCP	3,4,6,7,26,27,30,32,82
+3VS		+3VS	16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

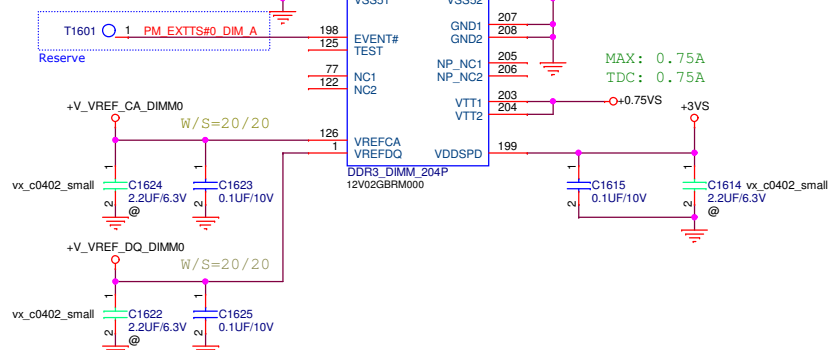
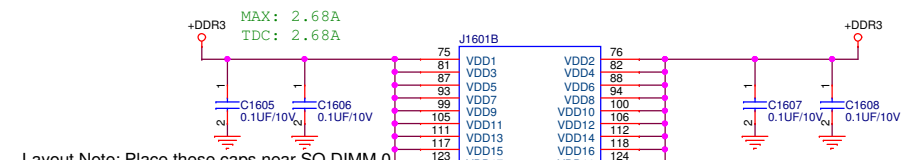
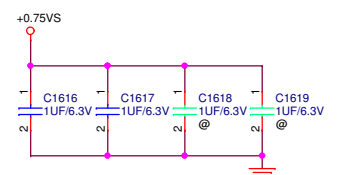
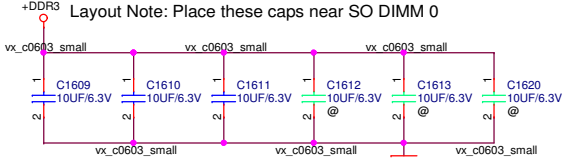
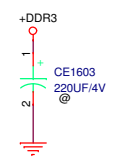
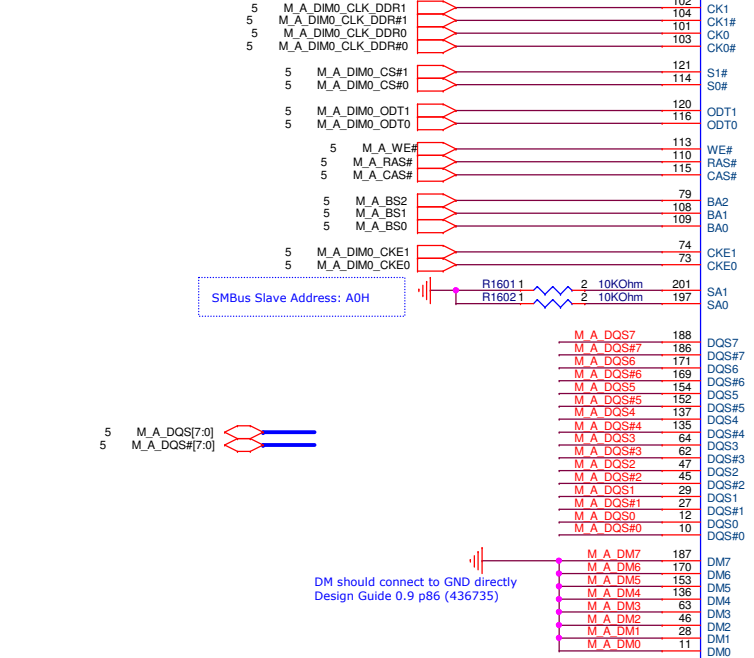
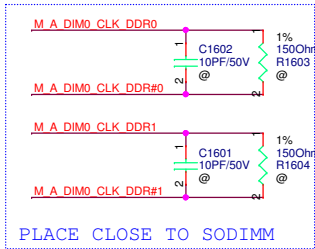
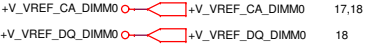
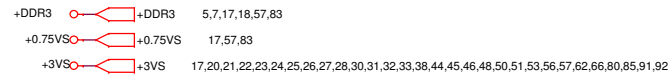
CPU XDP connector **Check Connector**

PCH XDP connector

Chief River
Decoupling guide from Intel PDDG R0.8
+VCORE 2.2uF * 16 pcs
22uF * 12 pcs



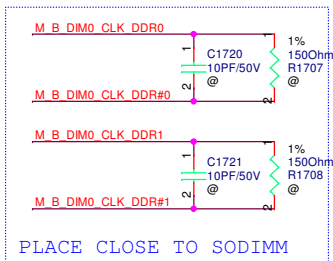
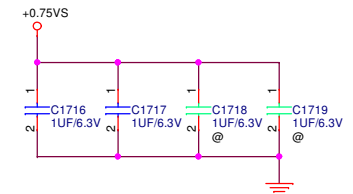
PEGATRON		Title : CPU DECOUPLING	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Trunks Chen	
Size B	Project Name B34		Rev 1.0
Date: Wednesday, February 01, 2012		Sheet	11 of 59



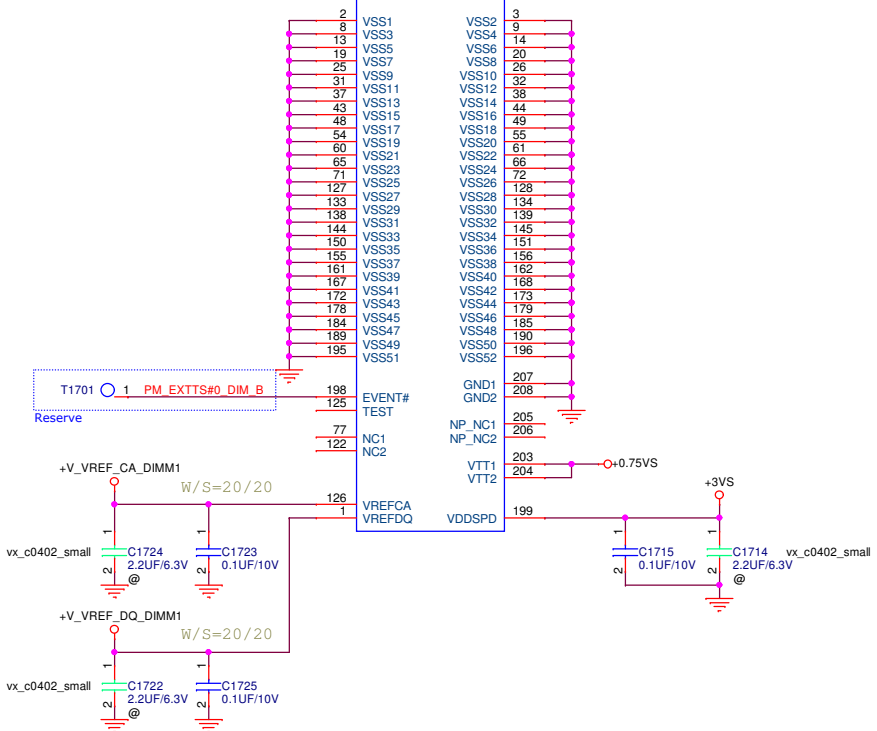
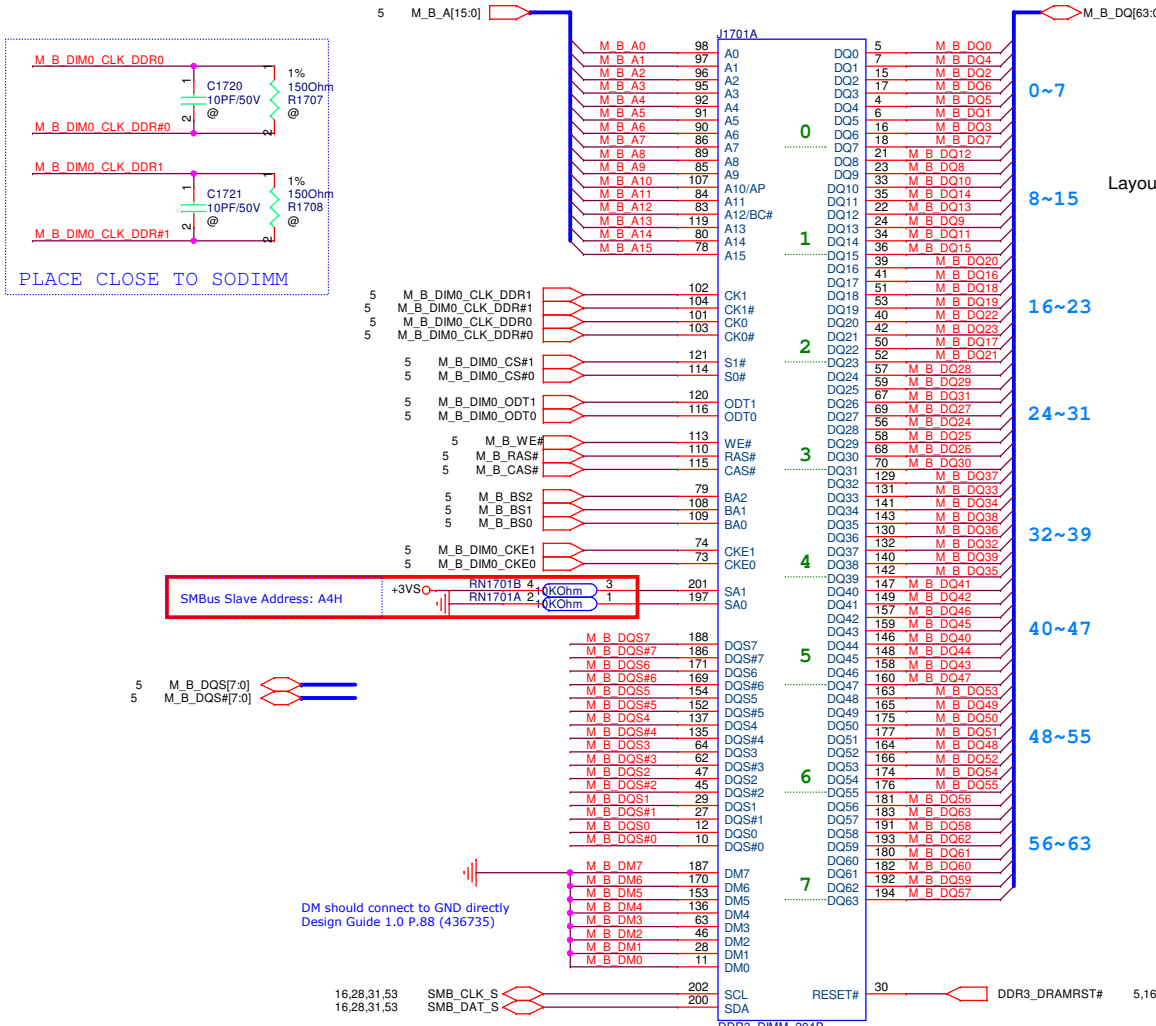
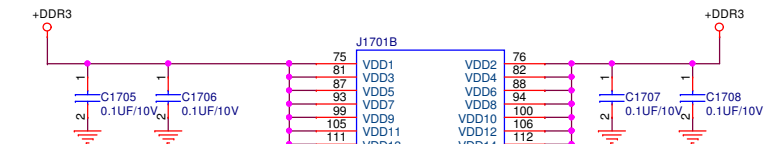
12V02GBRM000

M:1202-00EE000

S:1202-00KB000



Layout Note: Place these caps near SO DIMM 1



12V02GWSM000 **M:1202-00FG000**
H:5.2mm **S:1202-00K8000**

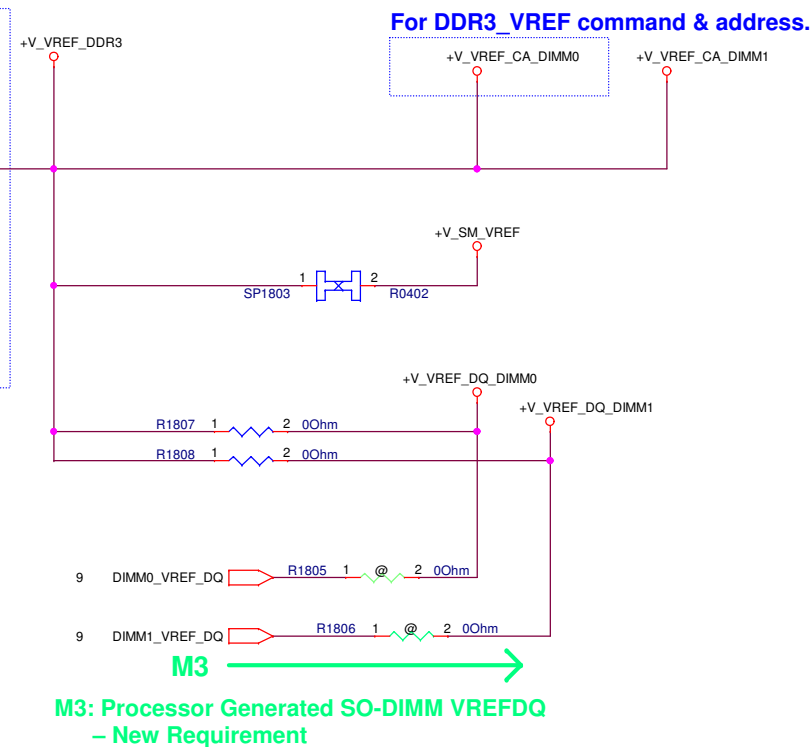
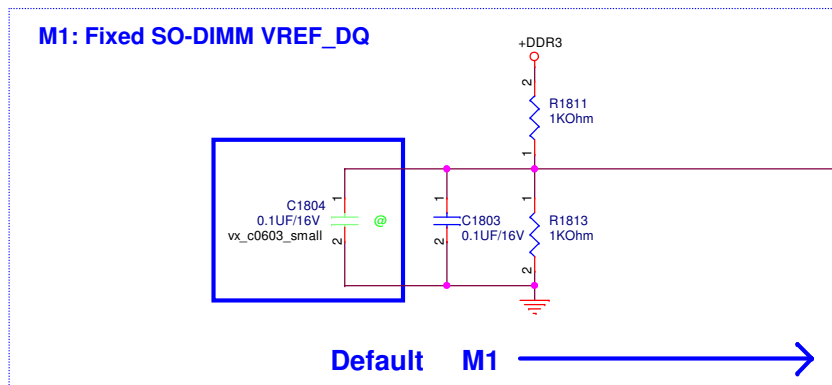
DDR3_DIMM_204F
12V02GWSM000

PEGATRON		Title : DDR3(2)_SO-DIMM1	
BGI\HW1		Engineer: <i>Trunks Chen</i>	
Size <i>Custom</i>	Project Name B34		Rev 2.1
Date: Wednesday, February 01, 2012		Sheet	17 of 98

DDR3 Vref

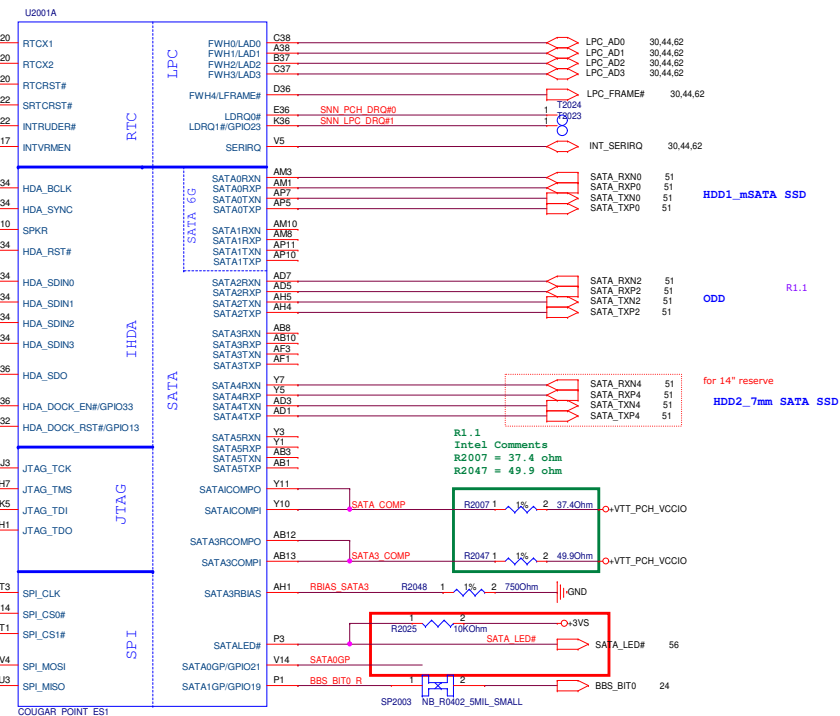
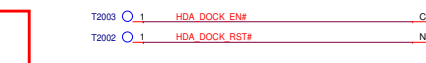
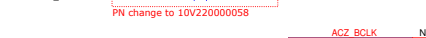
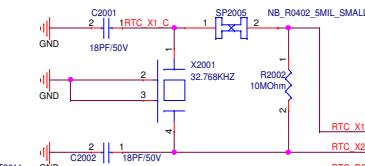
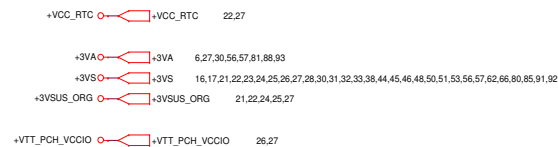
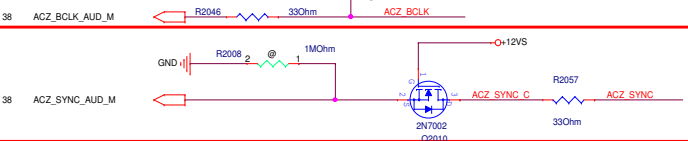
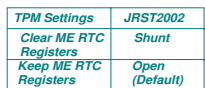
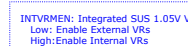
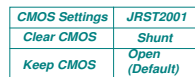
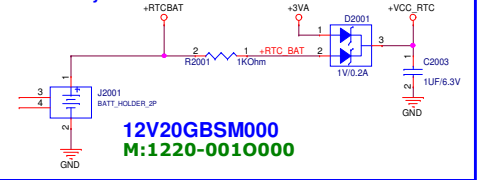
+DDR3 5,7,16,17,57,83
 +V_VREF_CA_DIMM0 16,17
 +V_VREF_DQ_DIMM0 16
 +V_SM_VREF 7,83

+3V 24,40,53,55,57,62,91
 +5VSUS 27,52,81,91
 +5VA 50,52,56,81



If support M3 :
 1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Un mount R1801,R1804

PEGATRON		Title :DDR3(3)_CA/DQ Voltage	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Trunks Chen	
Size B	Project Name B34		Rev 1.0
Date: Wednesday, February 01, 2012		Sheet	18 of 59

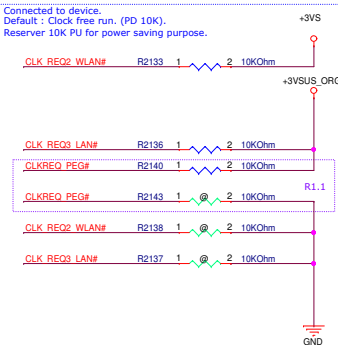
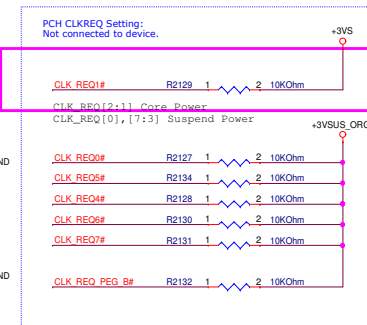
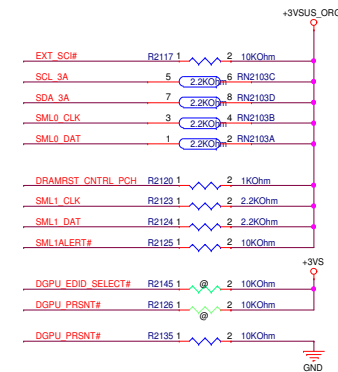
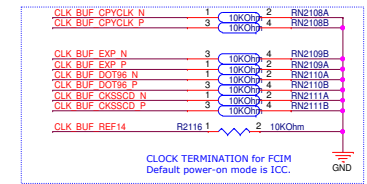
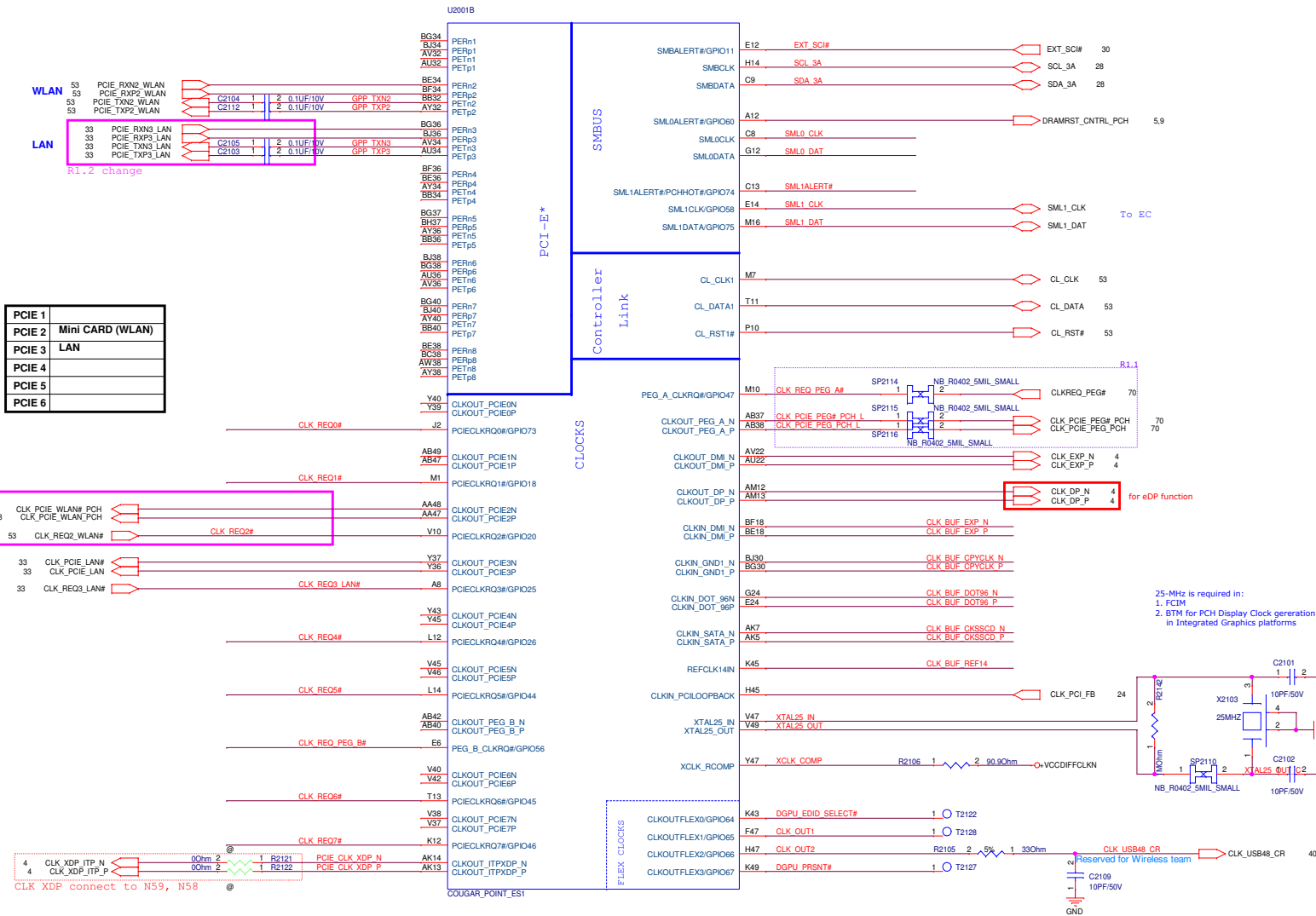


0200-00HU000 C.S 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH

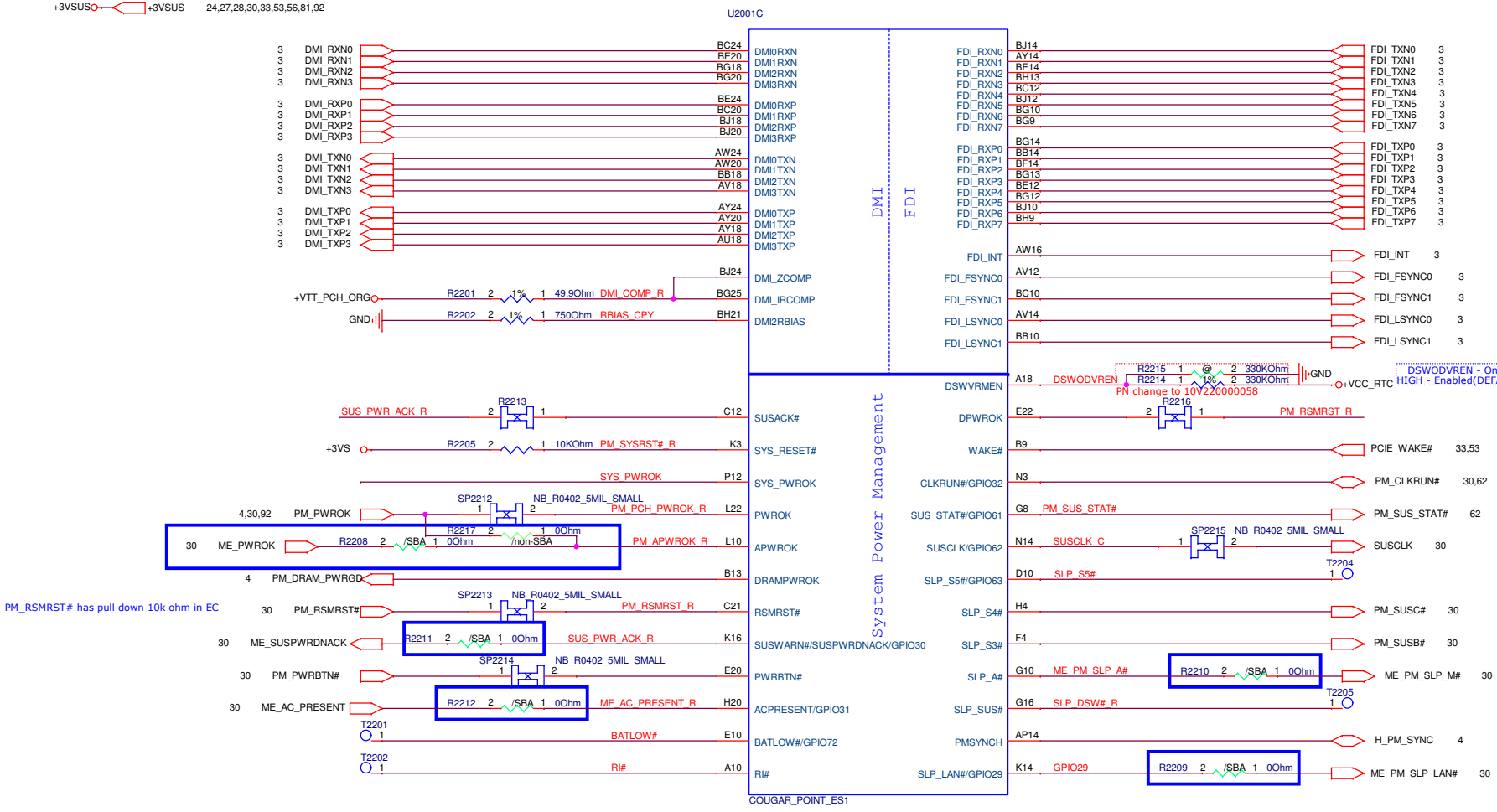
ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap



PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	LAN
PCIE 4	
PCIE 5	
PCIE 6	



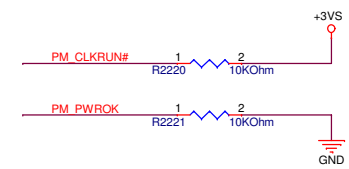
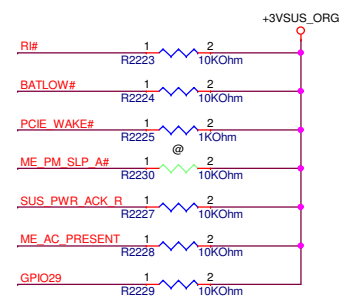
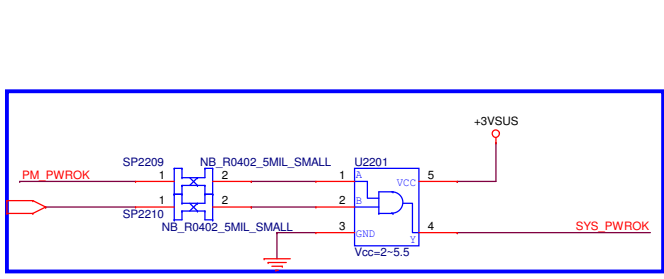
+3VSUS_ORG 20,21,24,25,27
+3VS 16,17,20,21,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+VTT_PCH_ORG 26,27
+3VA 6,20,27,30,56,57,81,88,93
+VCC_RTC 20,27
+3VSUS 24,27,28,30,33,53,56,81,92

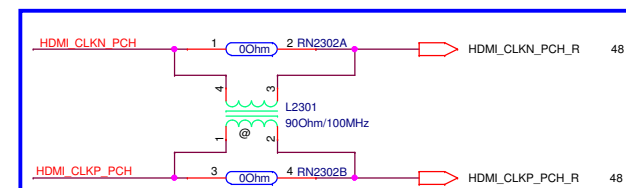
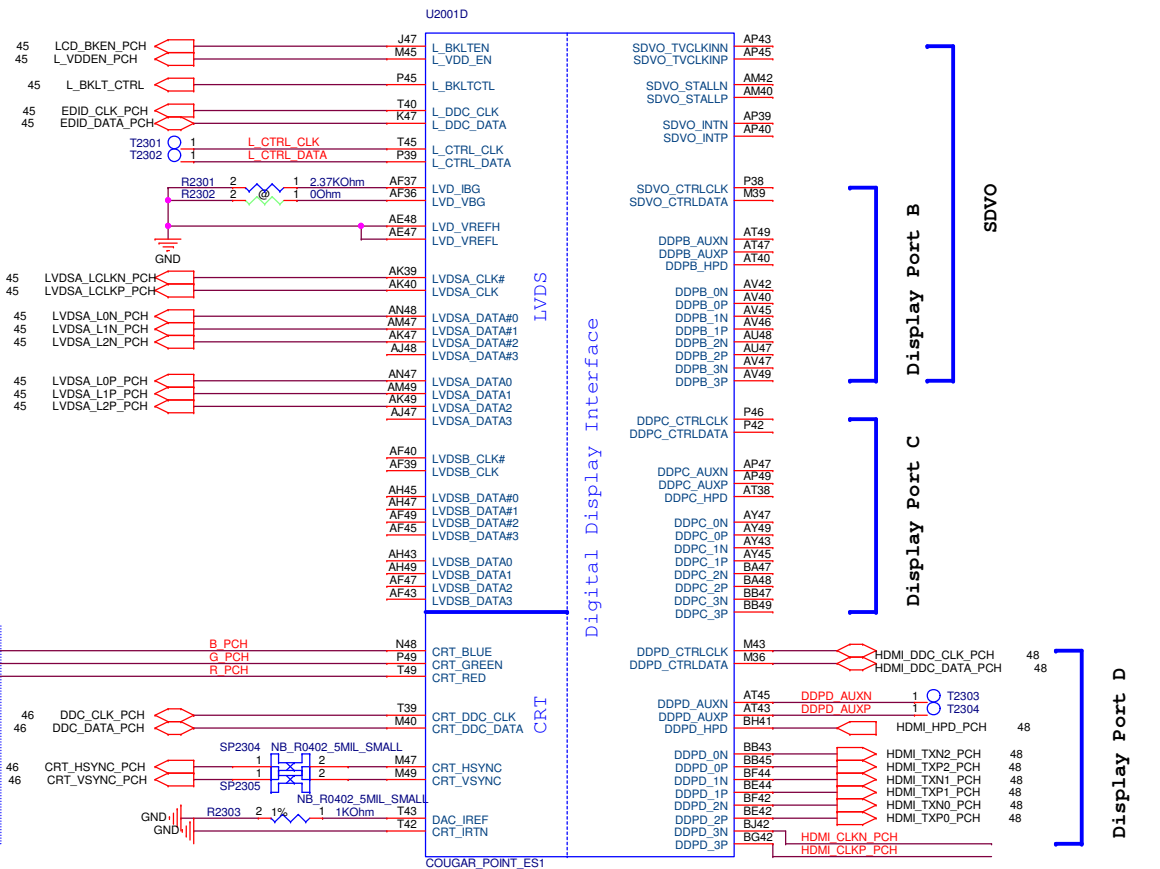
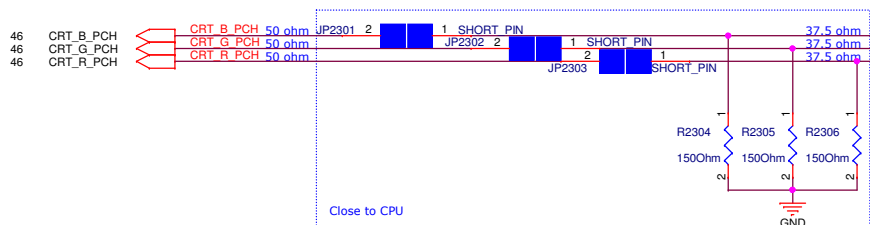
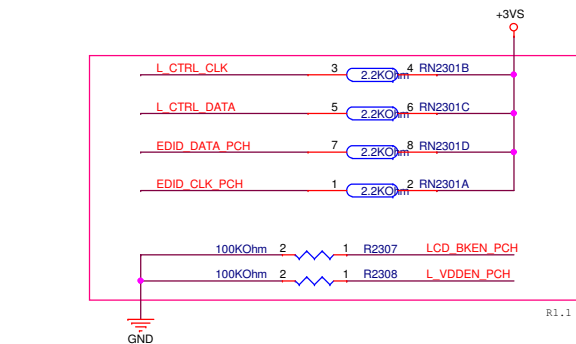


PM_RSMRST# has pull down 10k ohm in EC

DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW - Disabled

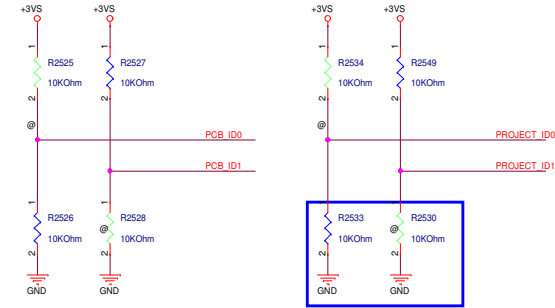
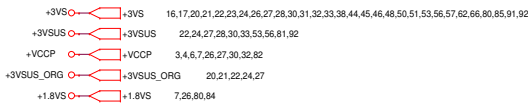
92 DELAY_VR_AND_ALL_SYS





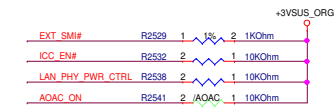
- 1. NC:**
CRT_RED,CRT_GREEN,CRT_BLUE
CRT_HSYCN,CRT_VSYNC
- 2. 1-k Ω \pm 0.5% pull-down to GND:**
DAC_IREF
- 3. Connected to GND:**
CRT_ITRN
- 4. Connect to +V3.3:**
VCCADAC

1. NC:
ALL

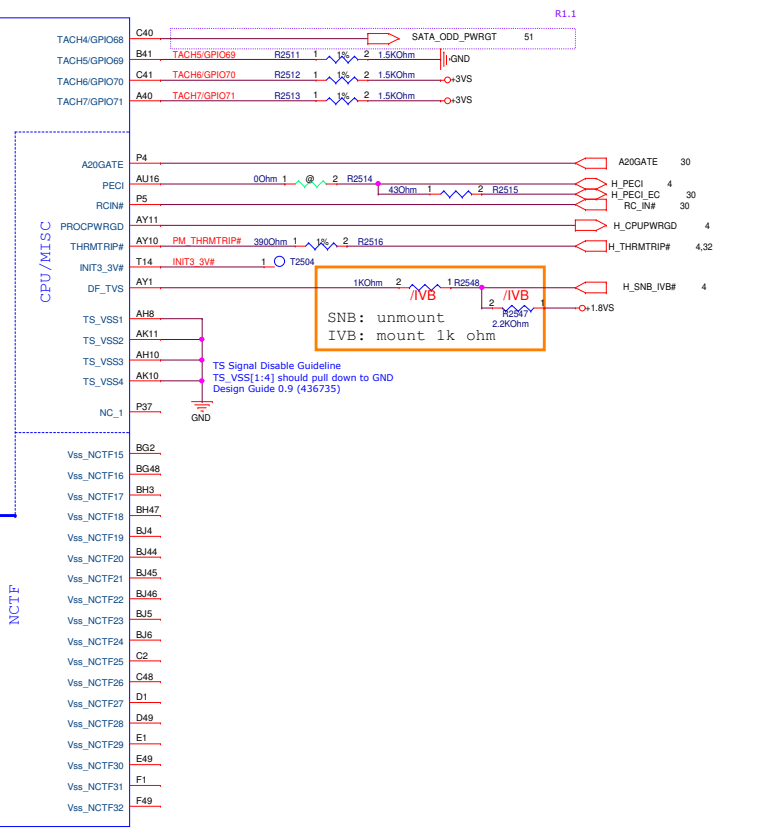
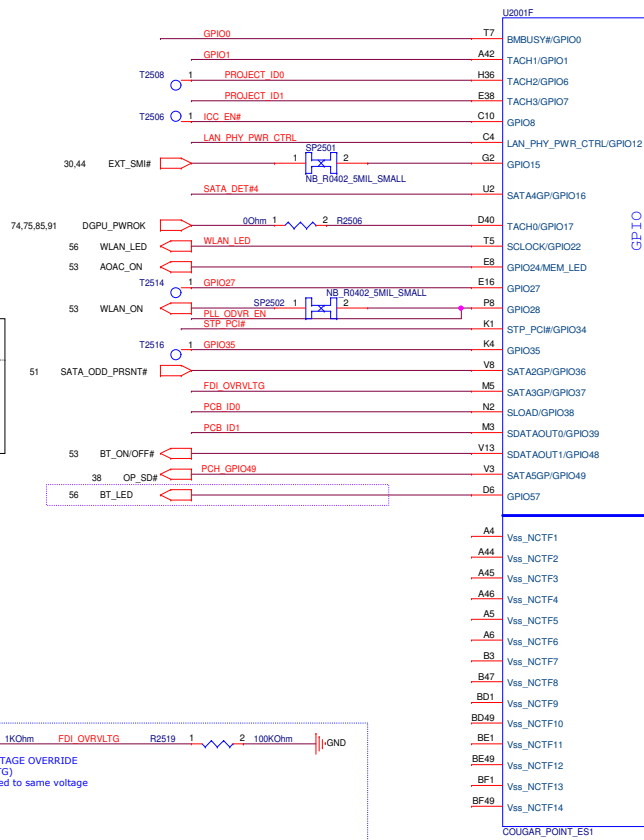
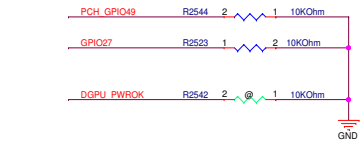
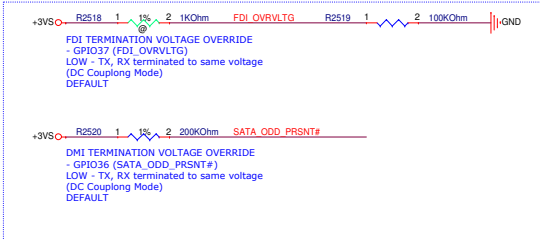
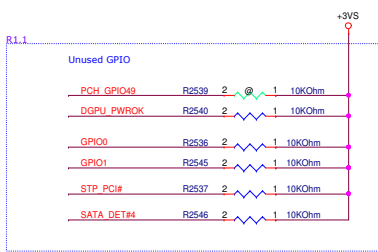


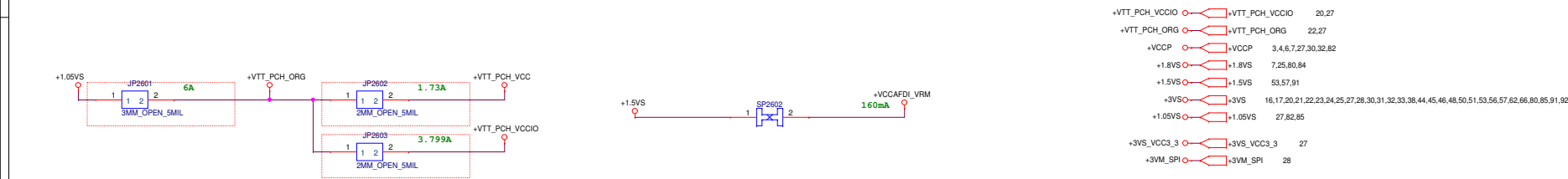
ID0	ID1	PCB Rev.
0	0	R1.1 (SR)
0	1	R1.2 (ER)
1	0	R2.0
1	1	R2.1











PROJECT_ID0	PROJECT_ID1	Model
0	0	B14 (UMA)
0	1	B34 (UMA / N13P-GL)
1	0	B74 (UMA / N13P-GS)
1	1	X

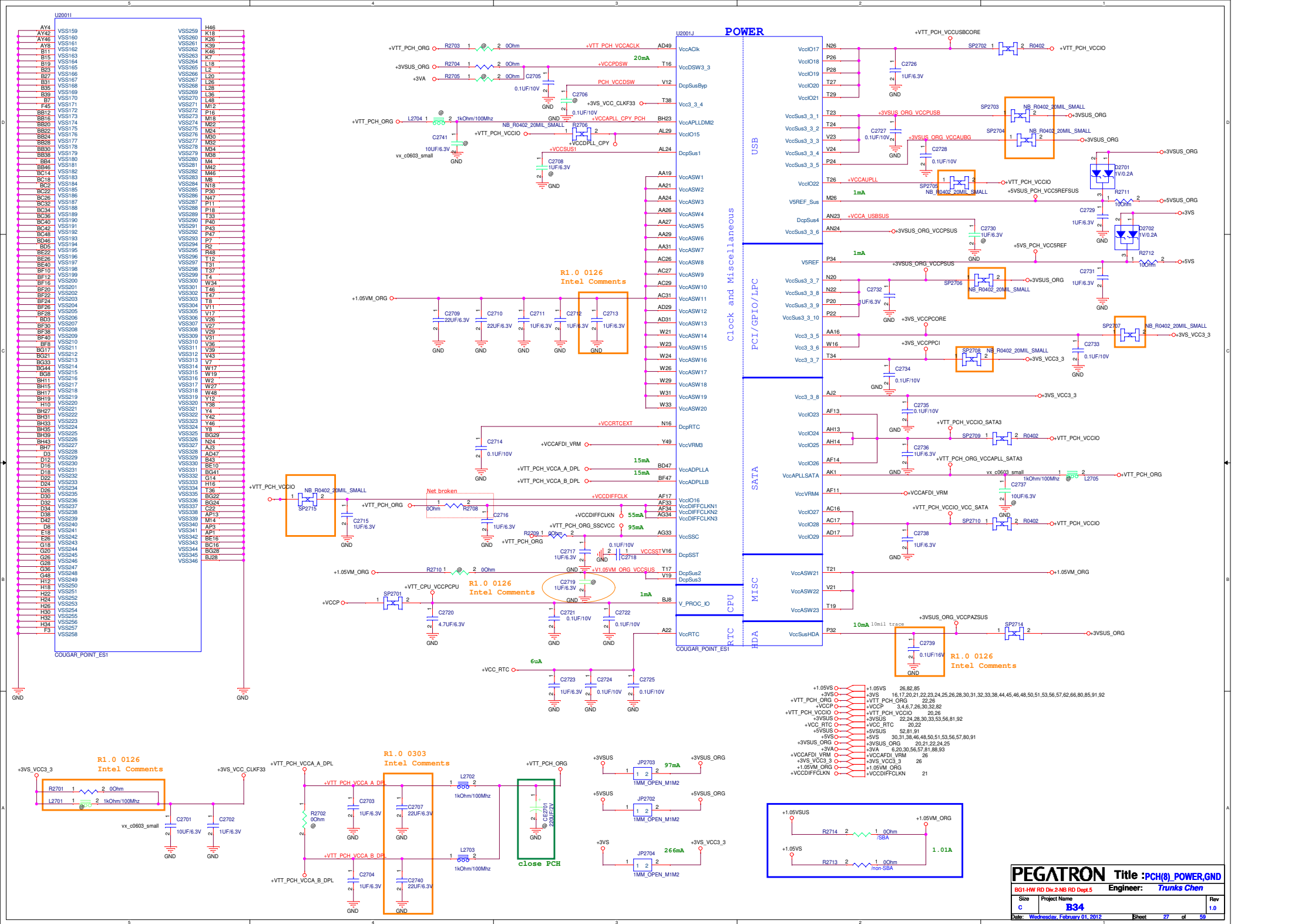


RCIN# has pull high at EC side

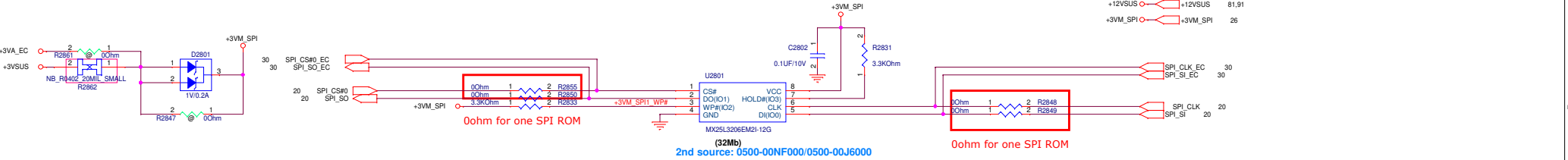




+VTT_PCH_VCCIO		+VTT_PCH_VCCIO	20,27
+VTT_PCH_ORG		+VTT_PCH_ORG	22,27
+VCCP		+VCCP	3,4,6,7,27,30,32,82
+1.8VS		+1.8VS	7,25,80,84
+1.5VS		+1.5VS	53,57,91
+3VS		+3VS	16,17,20,21,22,23,24,25,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+1.05VS		+1.05VS	27,82,85
+3VS_VCC3_3		+3VS_VCC3_3	27
+3VM_SPI		+3VM_SPI	28
+VCCAFDI_VRM		+VCCAFDI_VRM	27



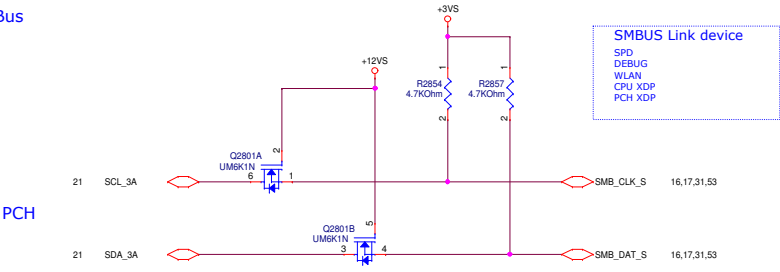
PCH SPI ROM

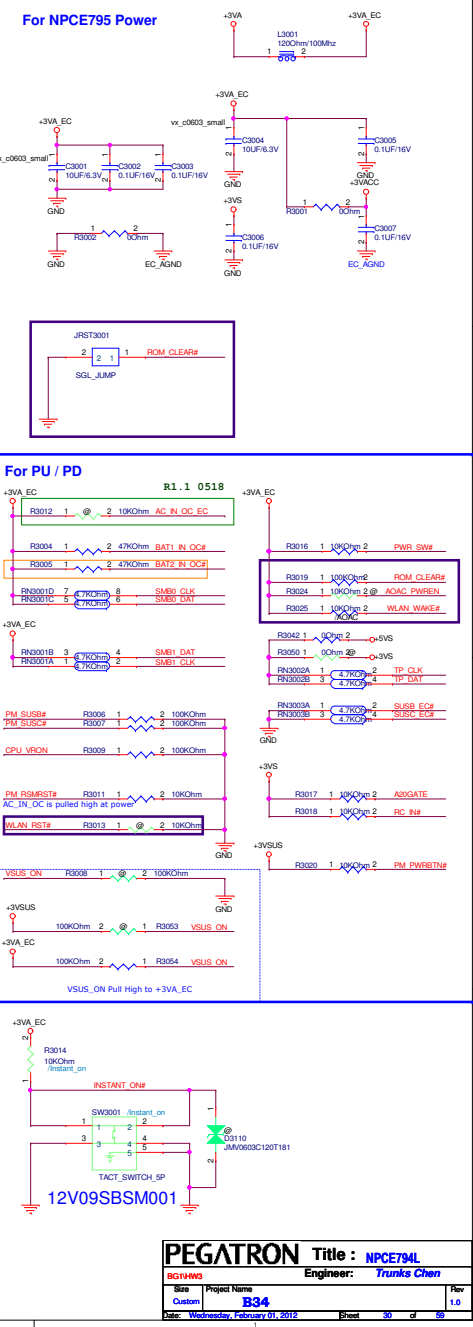
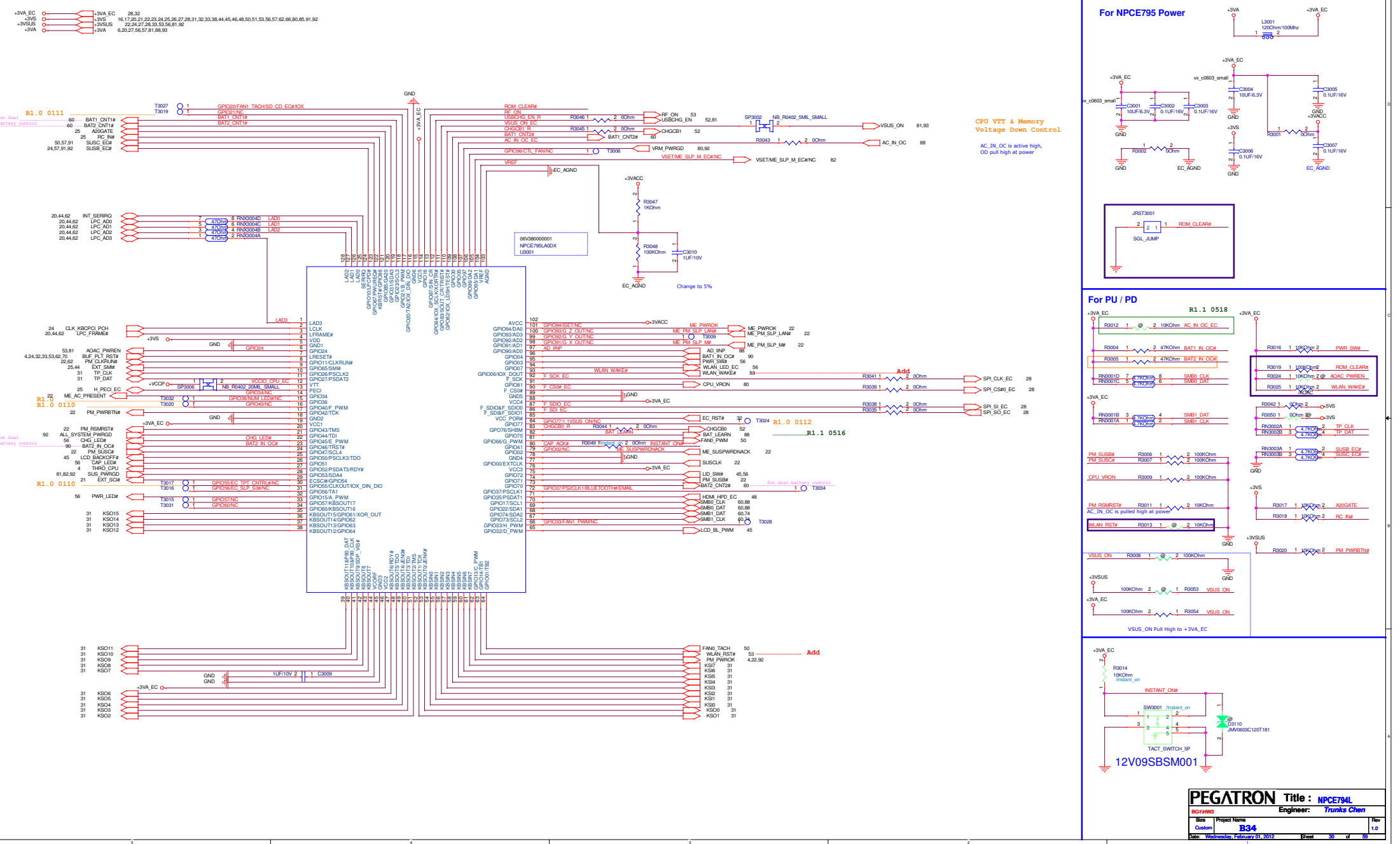


SPI Debug Connector

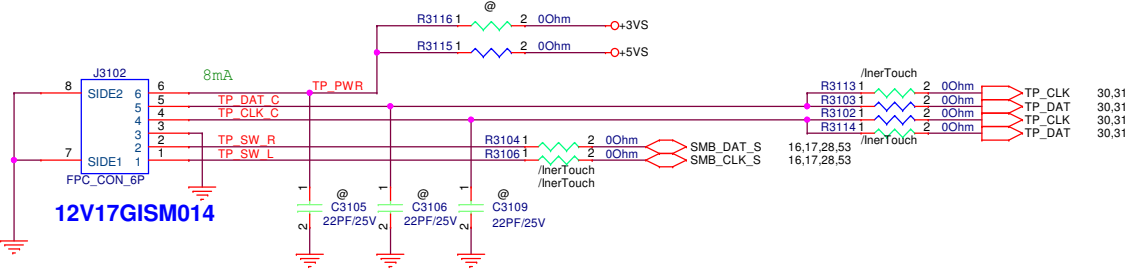
remove SPI connector

PCH SMBus

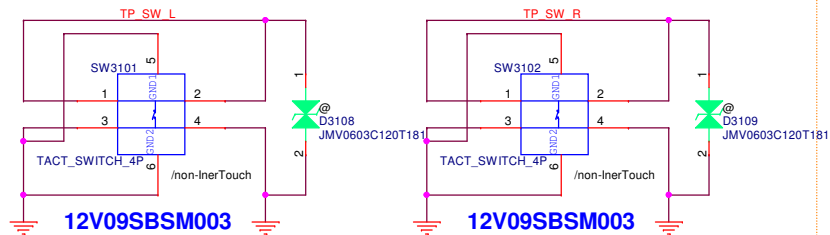




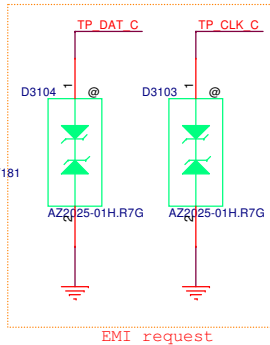
Touch Pad for inter touch & clear pad



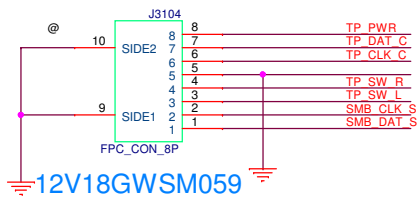
M:1218-00C7000
S:1218-00W8000



M:1209-00EQ000
S:1209-00EX000

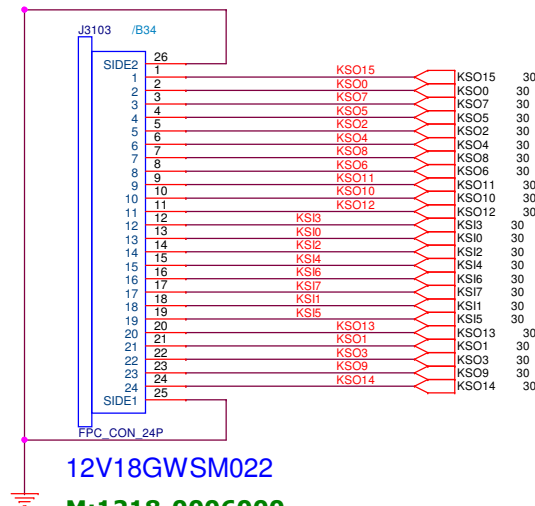


Touch Pad for inter touch & non- clear pad

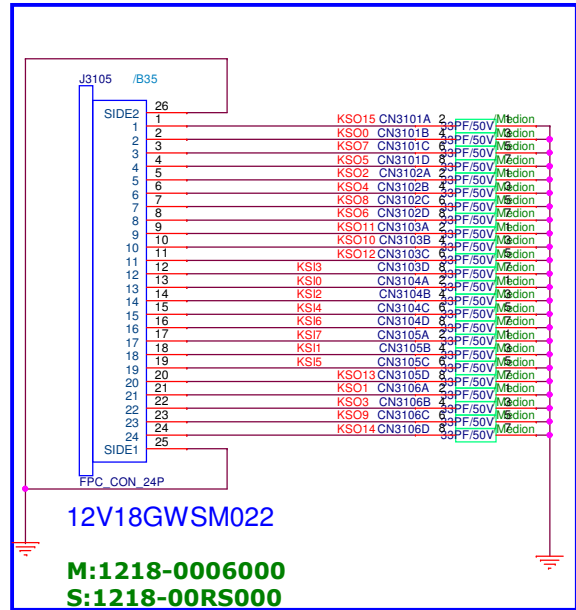


M:1218-006X000
S:1218-01JN000

Keyboard

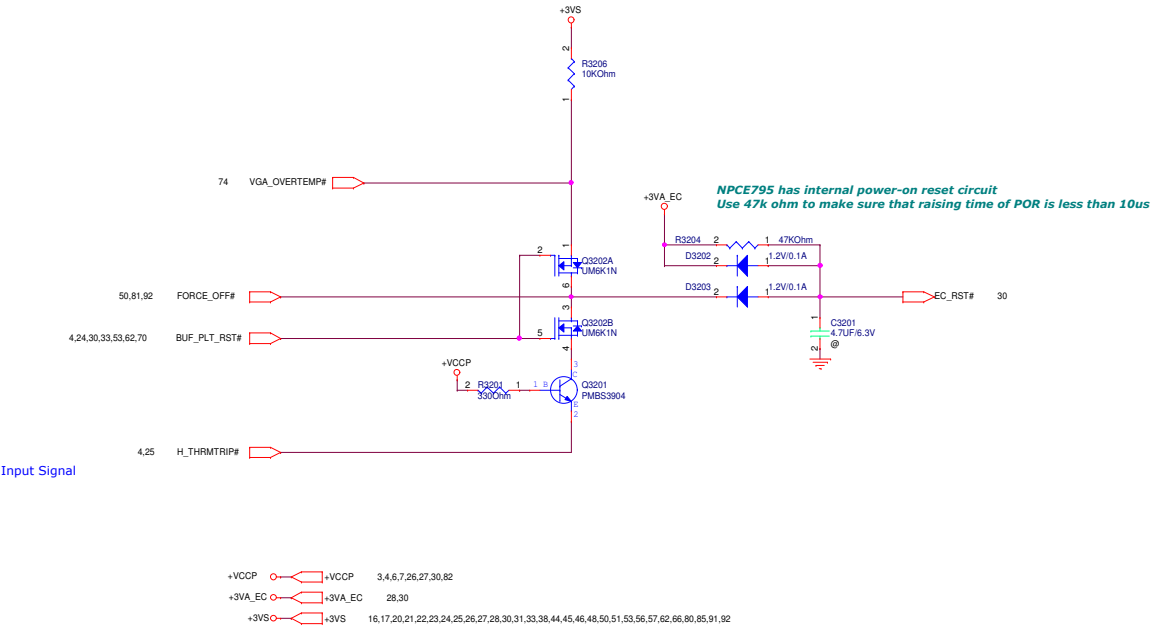


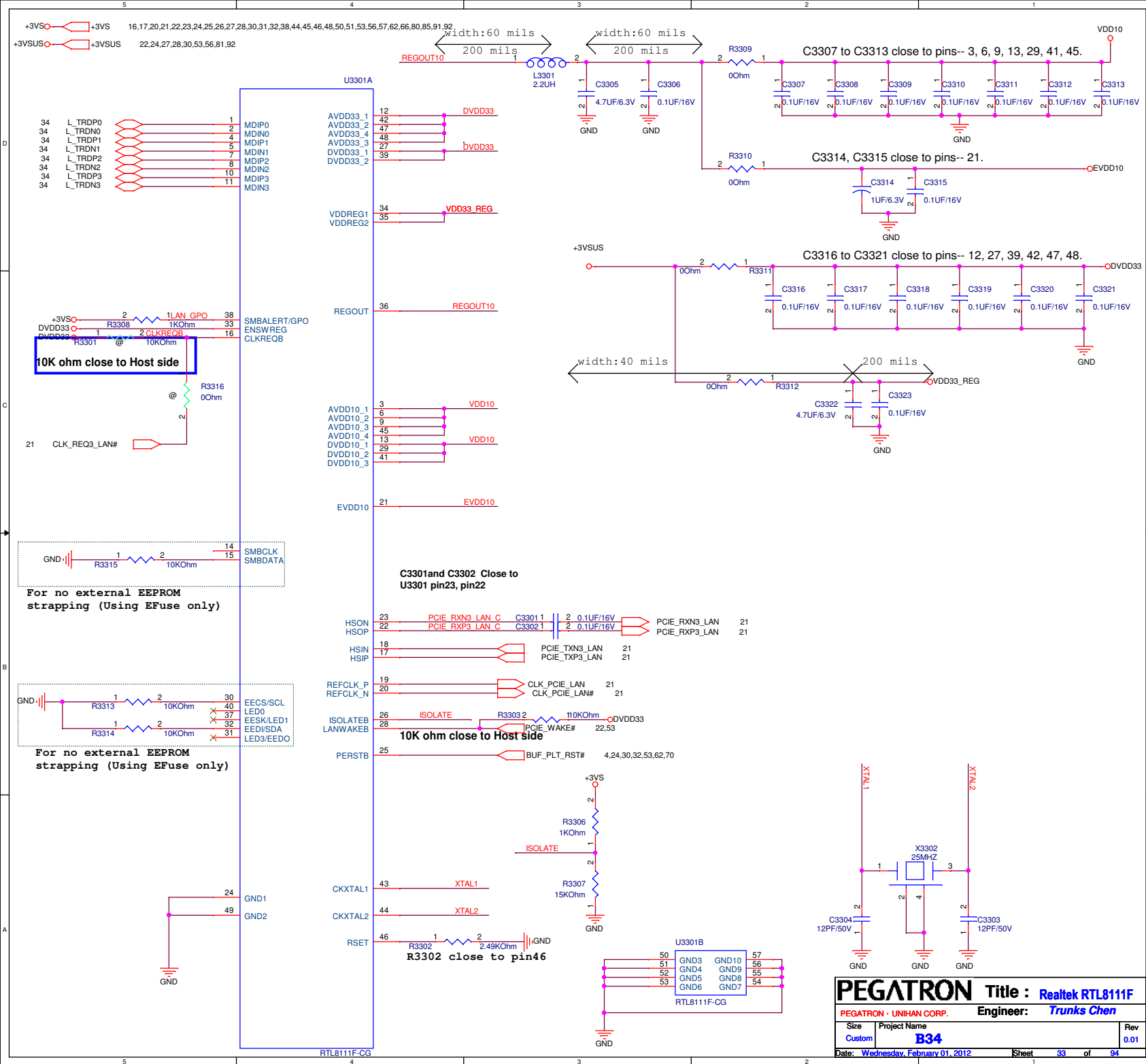
M:1218-0006000
S:1218-00RS000

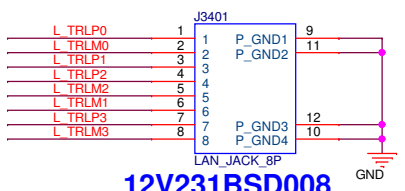
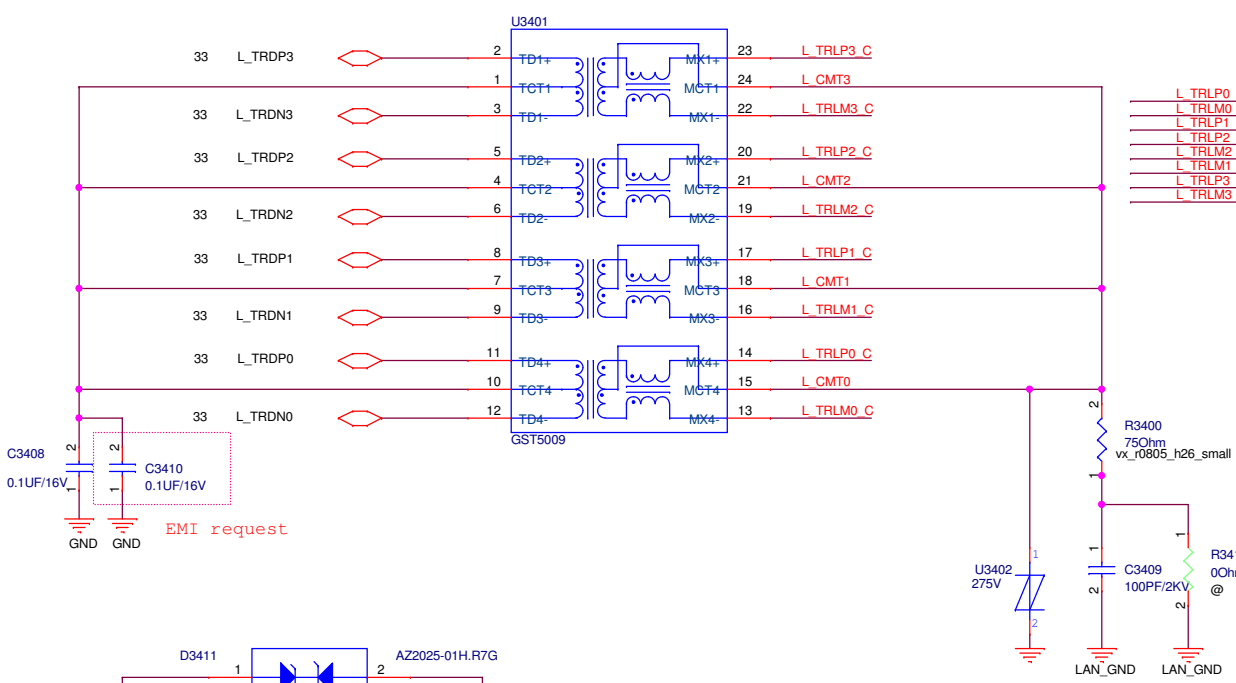


M:1218-0006000
S:1218-00RS000

Thermal Policy

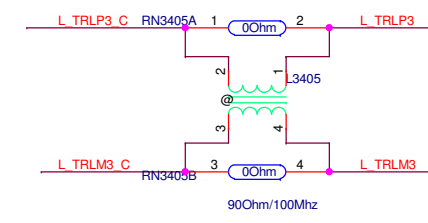
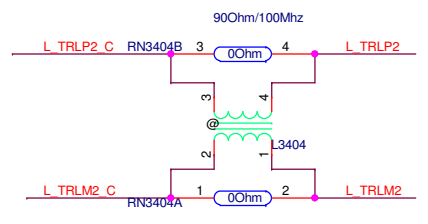
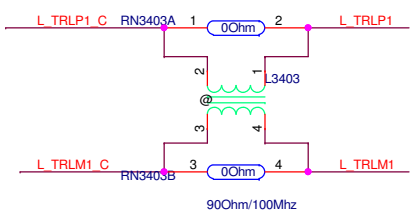
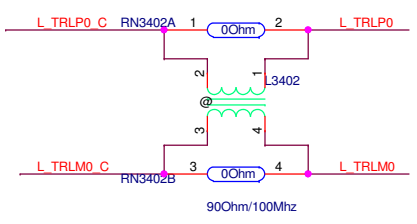
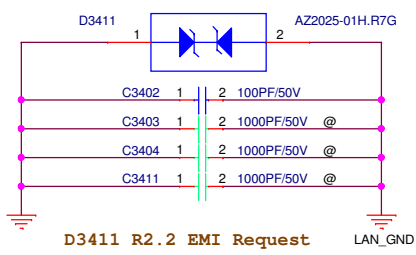
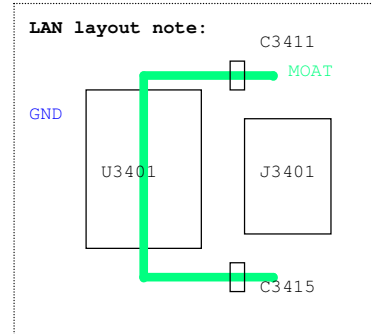


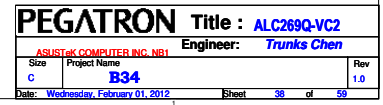




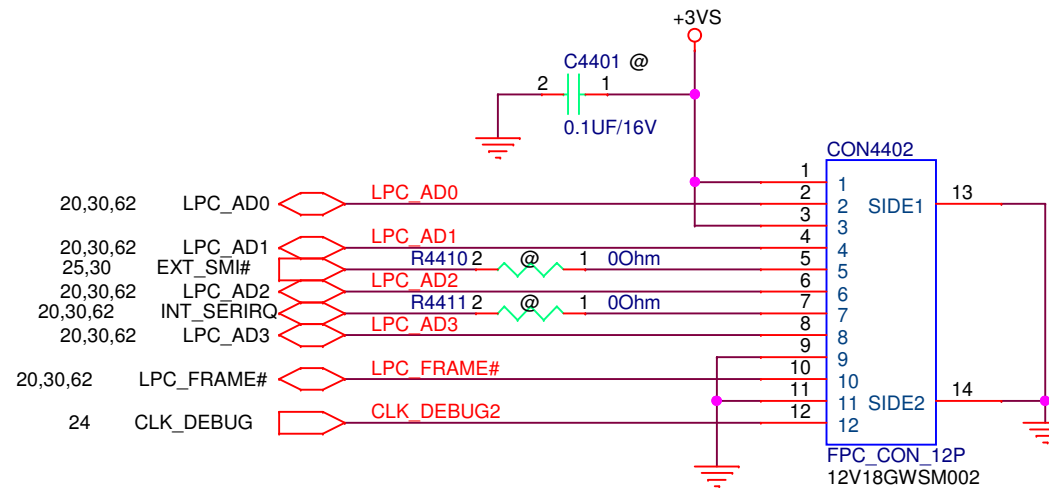
12V231BSD008

M:1223-00S4000
S:1223-00QS000



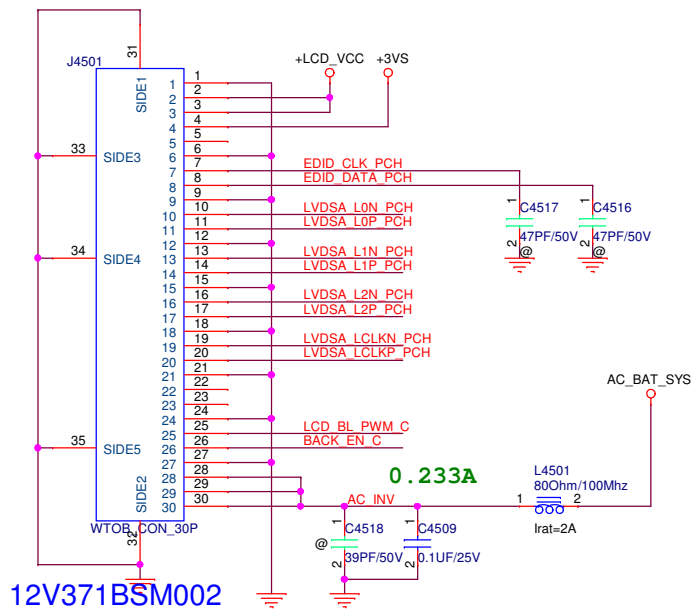


DEBUG CARD CONN.



PEGATRON		Title : BUG_Debug	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Trunks Chen	
Size A	Project Name B34		Rev 1.0
Date: Wednesday, February 01, 2012		Sheet 44 of 59	

LVDS Conn w/Camera Module

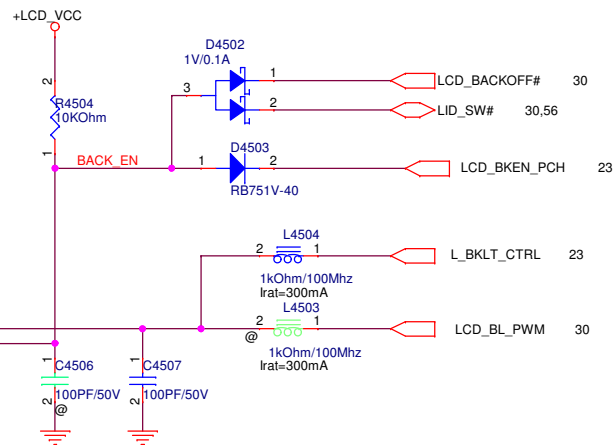
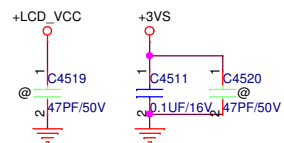


12V371BSM002

M:1237-0025000

S:1237-002A000

S:1237-002E000



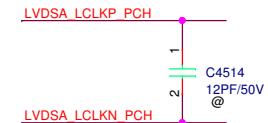
LVDSA_LCLKP_PCH 23
LVDSA_LCLKN_PCH 23

LVDSA_L0P_PCH 23
LVDSA_L0N_PCH 23

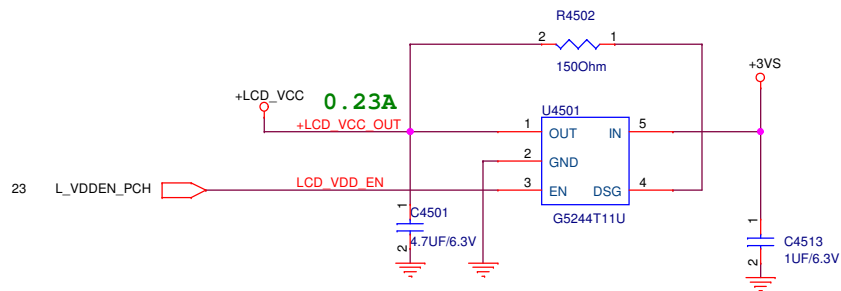
LVDSA_L1P_PCH 23
LVDSA_L1N_PCH 23

LVDSA_L2P_PCH 23
LVDSA_L2N_PCH 23




EDID_CLK_PCH 23
EDID_DATA_PCH 23



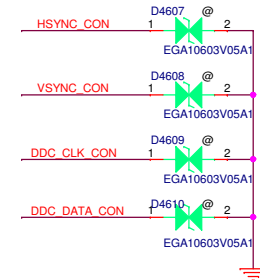
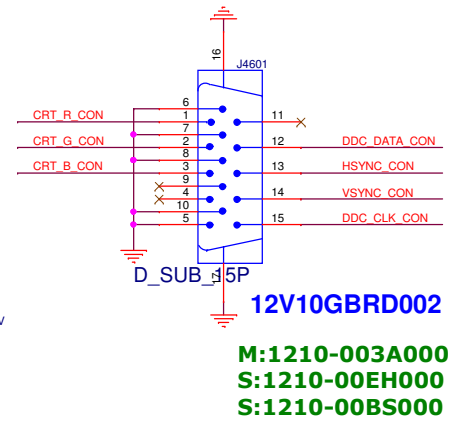
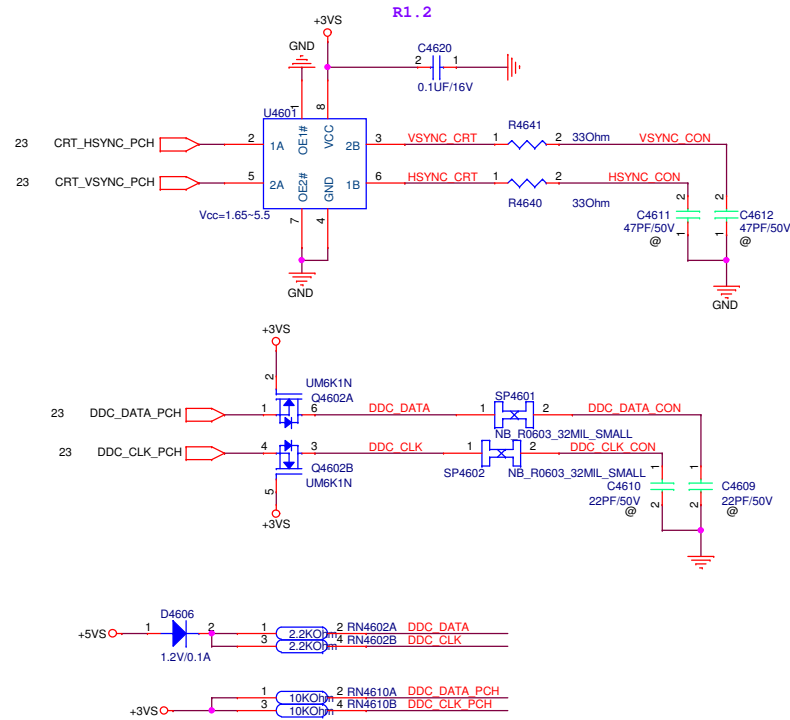
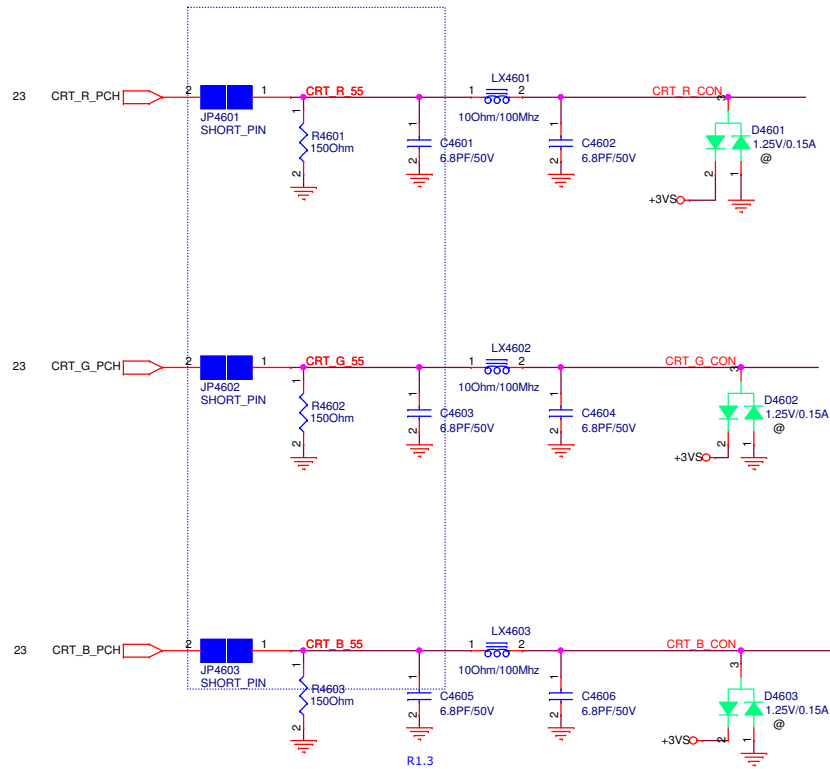
LCD VDDEN / +LED_VCC



PEGATRON			Title : LVDS CONN	
BG1-HW RD Div.2-NB RD Dept.5			Engineer: Trunks Chen	
Size B	Project Name B34			Rev 1.0
Date: Wednesday, February 01, 2012		Sheet 45 of 59		

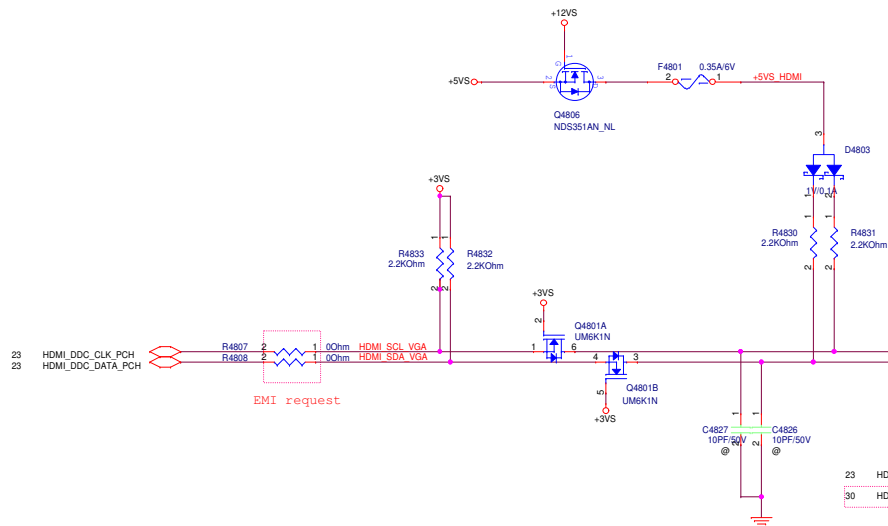
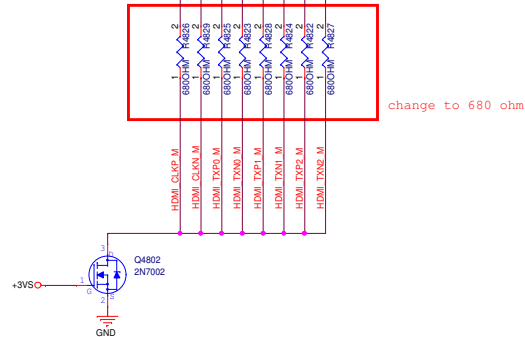
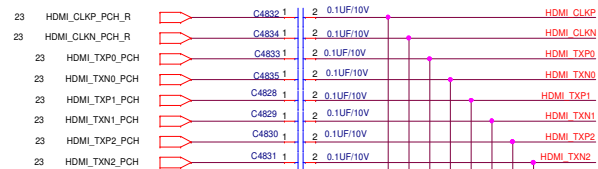
+3VS  +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,48,50,51,53,56,57,62,66,80,85,91,92
+5V  +5V 52,55,56,57,66,91
+5VS  +5VS 27,30,31,38,48,50,51,53,56,57,80,91

Change to NV optimus solution

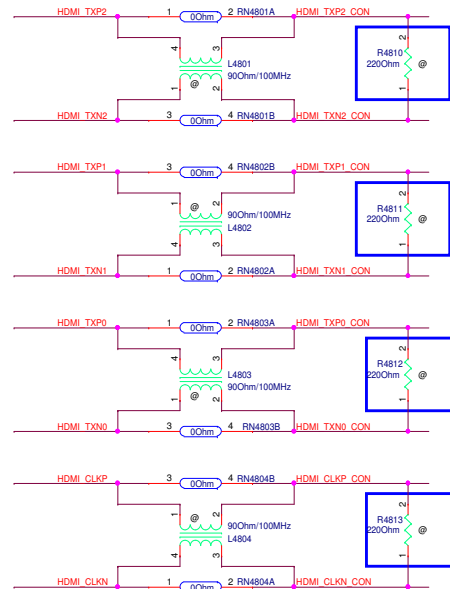


PEGATRON		Title : CRT(2) D-Sub	
BG11HW1		Engineer: Trunks Chen	
Size Custom	Project Name B34	Rev 2.1	
Date: Wednesday, February 01, 2012			
		Sheet	46 of 98

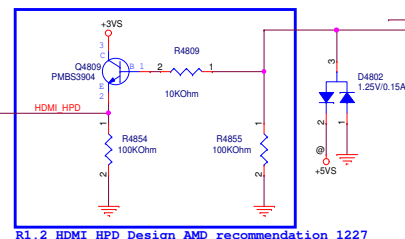
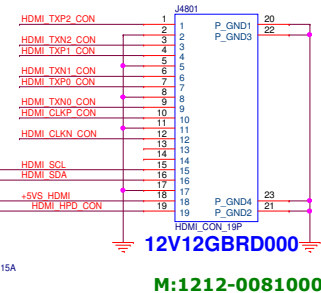
+12VS +12VS 20,28,91
+3VS +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,50,51,53,56,57,62,66,80,85,91,92
+5VS +5VS 27,30,31,38,46,50,51,53,56,57,80,91



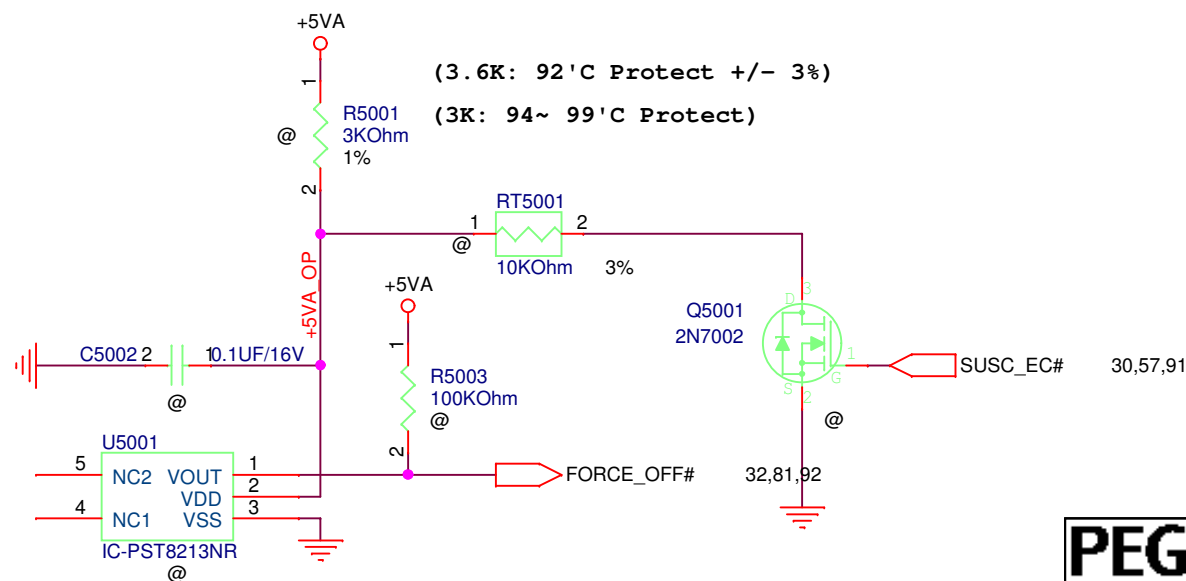
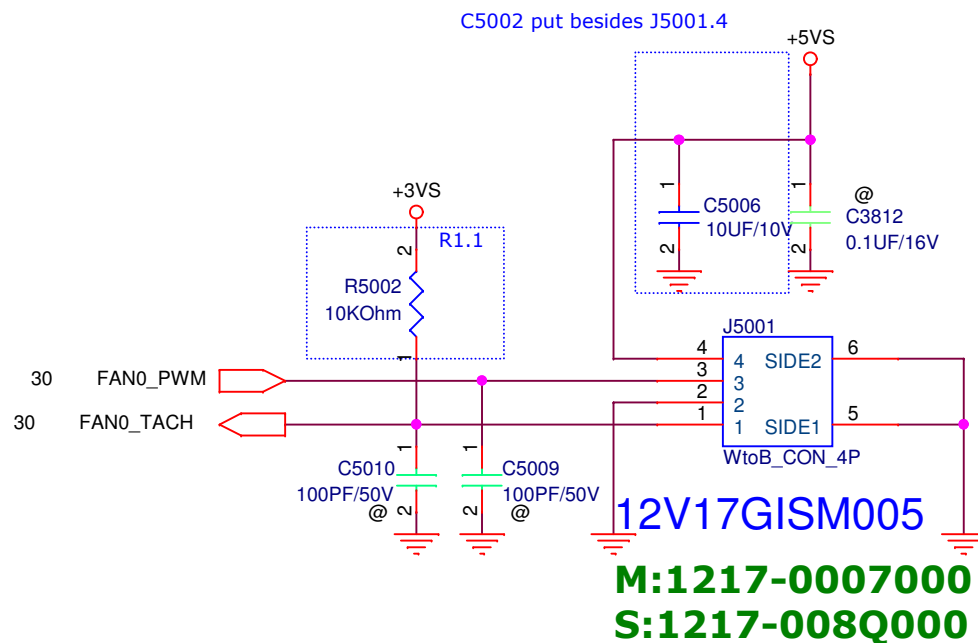
HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible



R1.2 for EMI solution
R4810-R4813



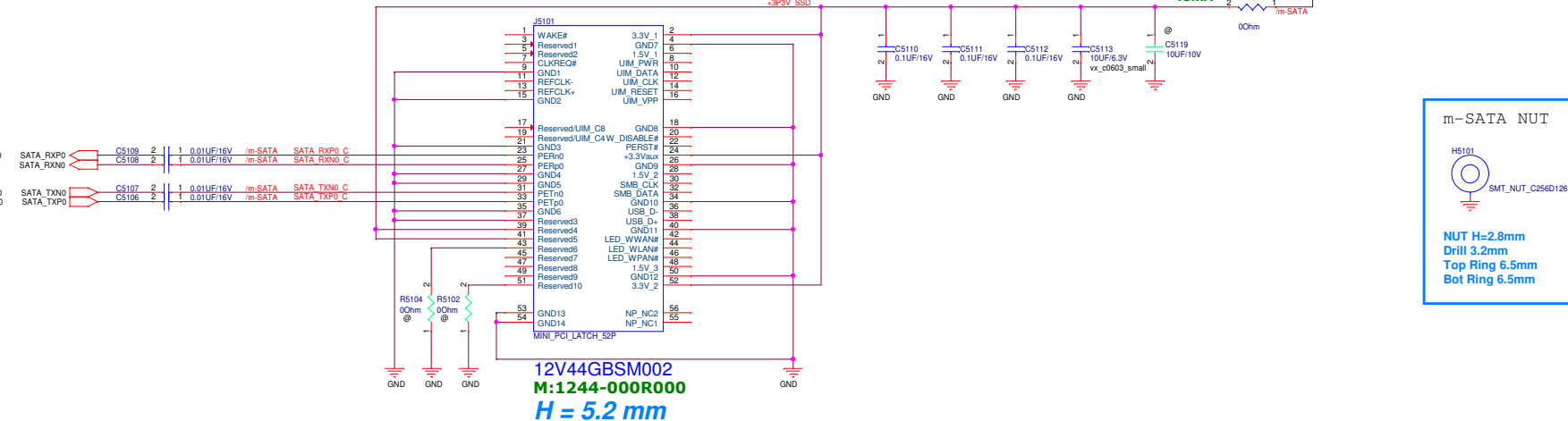
PWM Fan



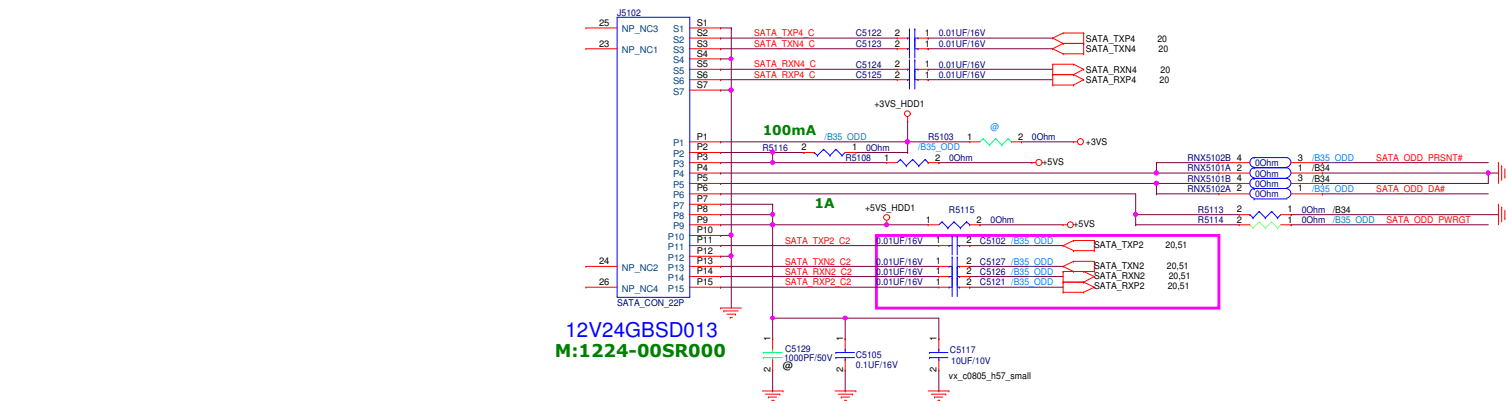
PEGATRON		Title : THERMAL/ FAN	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Trunks Chen	
Size A	Project Name B34		Rev 1.0
Date: Wednesday, February 01, 2012		Sheet 50	of 59

mSATA SSD mini card connector

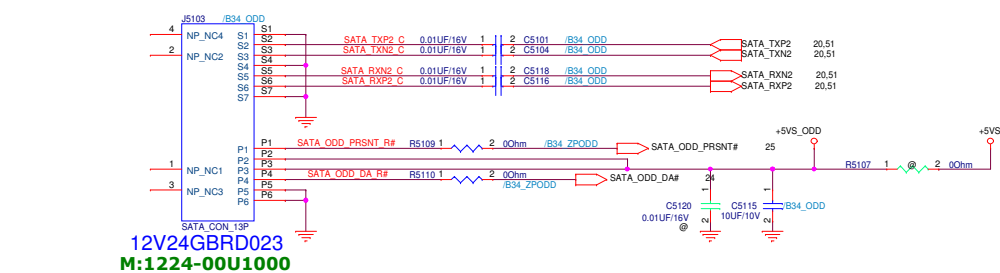
Need check pin definition



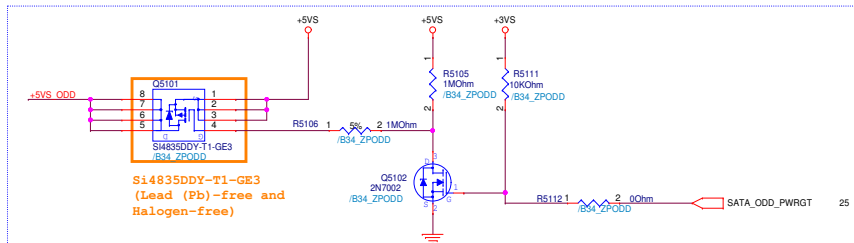
7mm SATA SSD connector



ODD

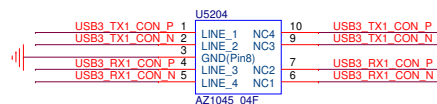
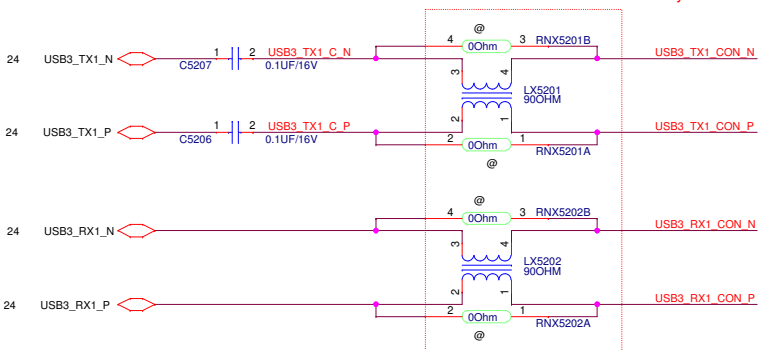


Zero Power ODD Support



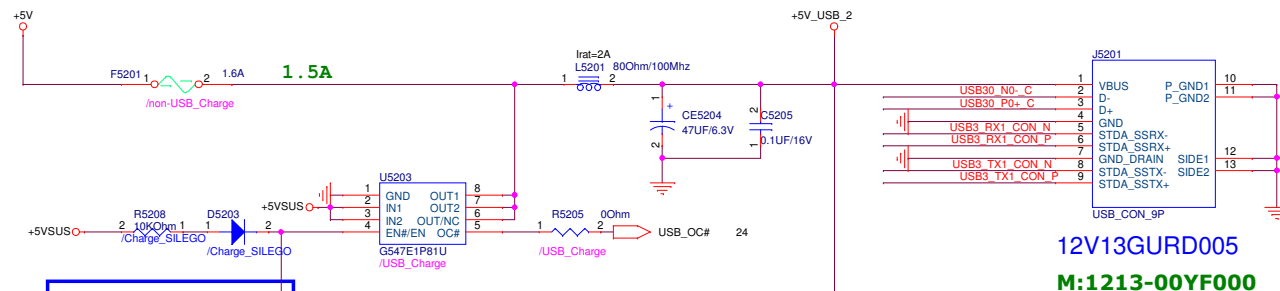
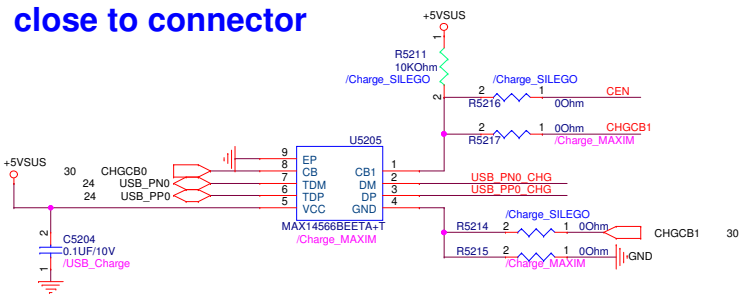
USB 3.0 & USB 2.0 Combo

RNX5201 RXN5202 ref. name modify



PLACE ESD Diodes near Connector

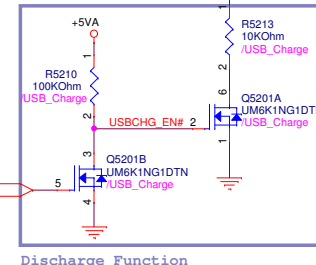
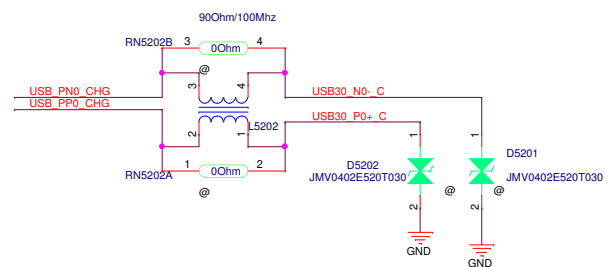
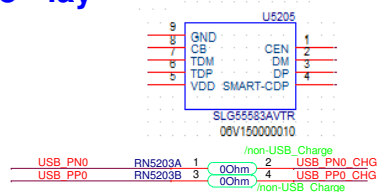
MAXIM USB Charger IC MAX14566BE close to connector



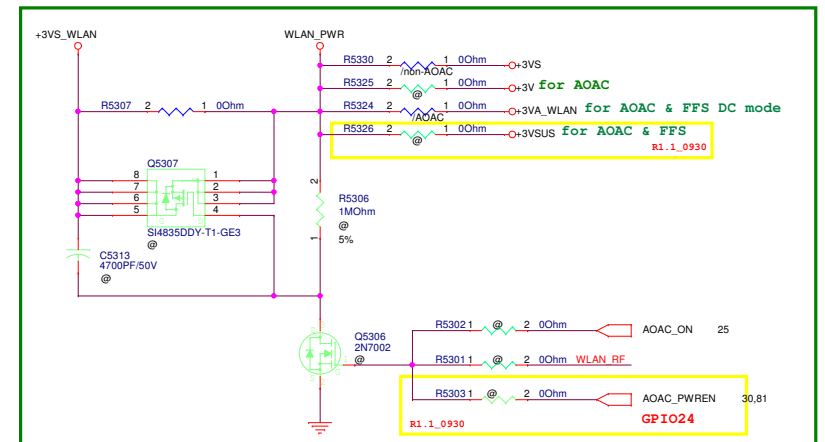
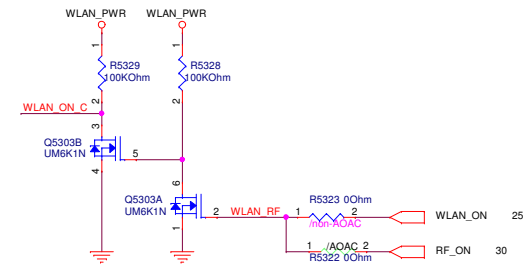
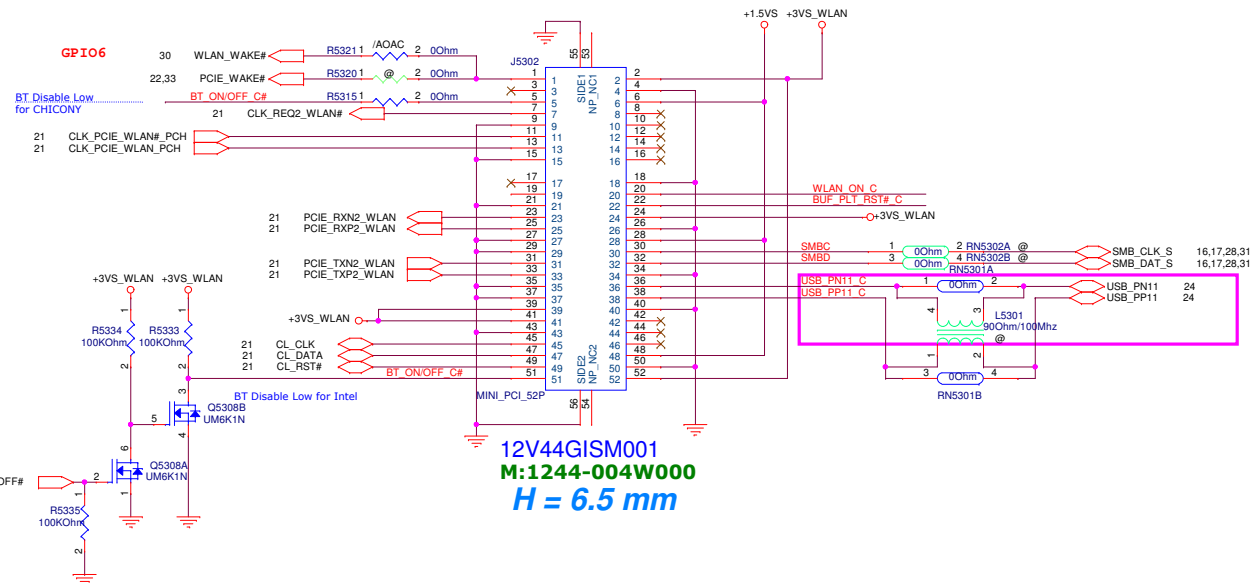
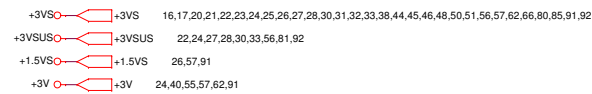
12V13GURD005
M:1213-00YF000

Optional

Co - lay SILEGO



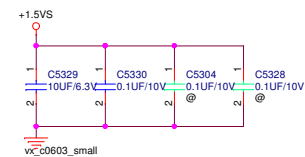
WLAN+BT/WiMax



WLAN +1.5VS bypass capacitor:

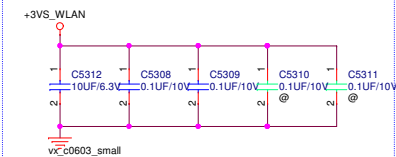
Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

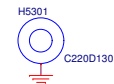


WLAN +3VS bypass capacitor:

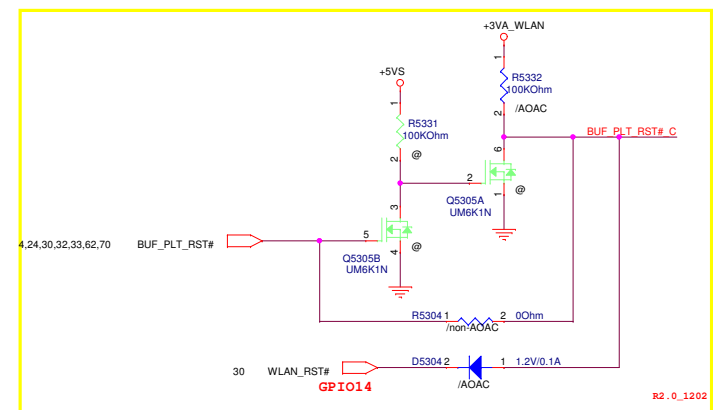
Place 0.1UF near pin 2,24,52,39 41.
Place 10UF near +3VS_WLAN source side.






WLAN NUT

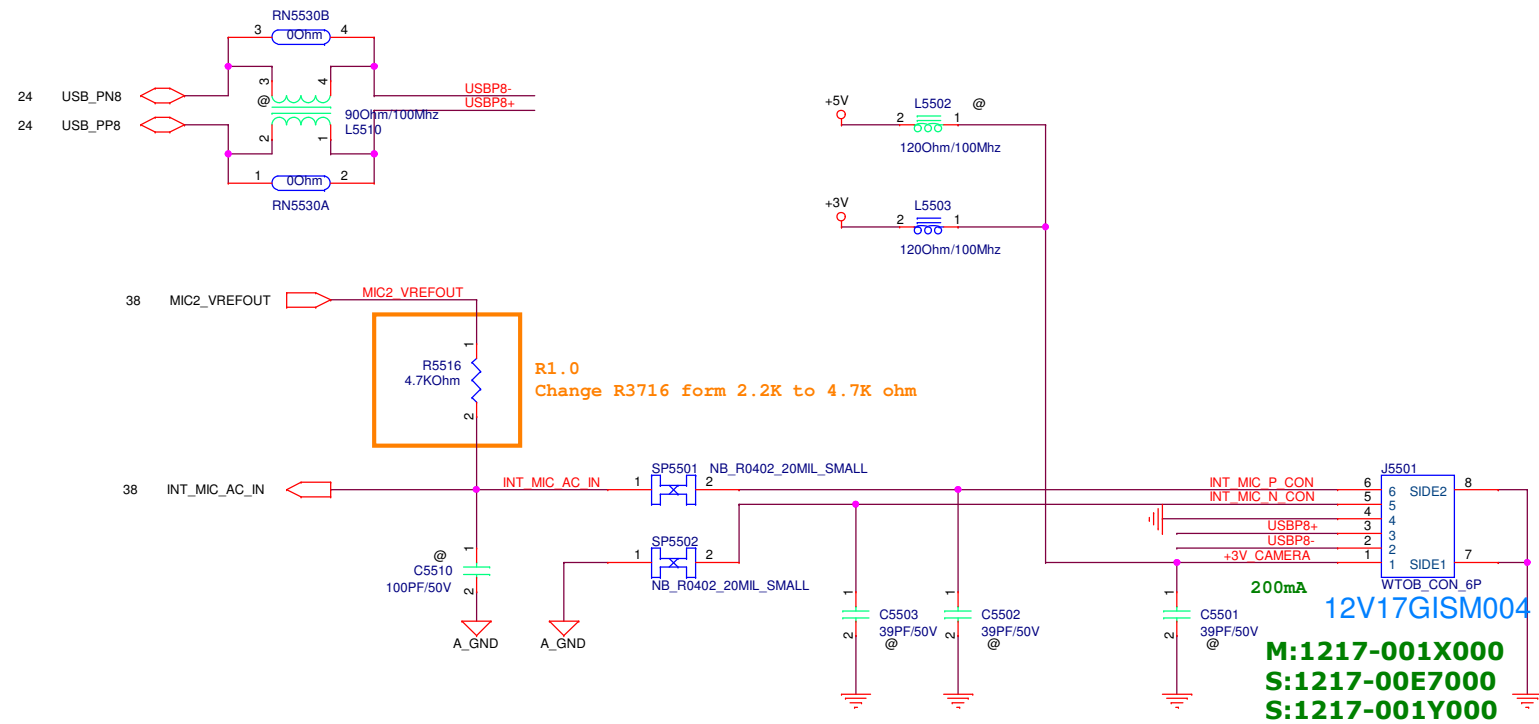


NUT H=4mm
Drill 3.3mm
Top Ring 5.5mm
Bot Ring 5.5mm

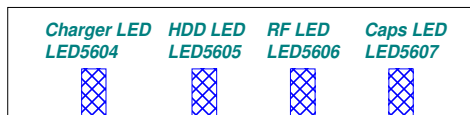


Camera

+3VS 	+3VS	16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+3V 	+3V	24,40,53,57,62,91
+5V 	+5V	52,56,57,66,91



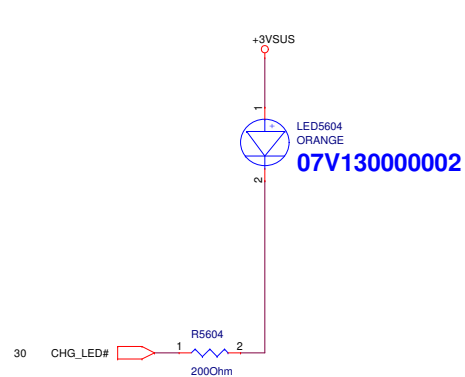
LED Side light



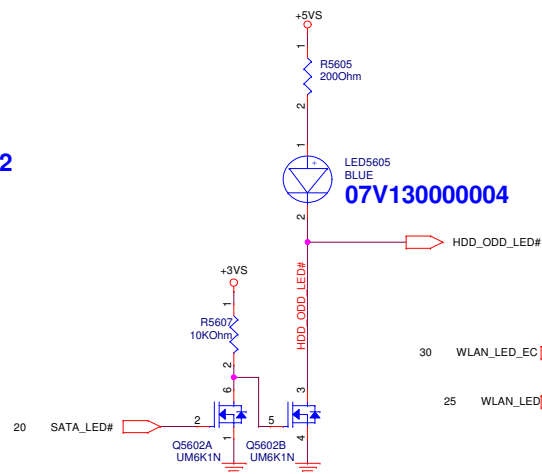
LED Placement
Left-->Right

Order of Indicator LEDs
Battery HDD/ODD WiFi Caps

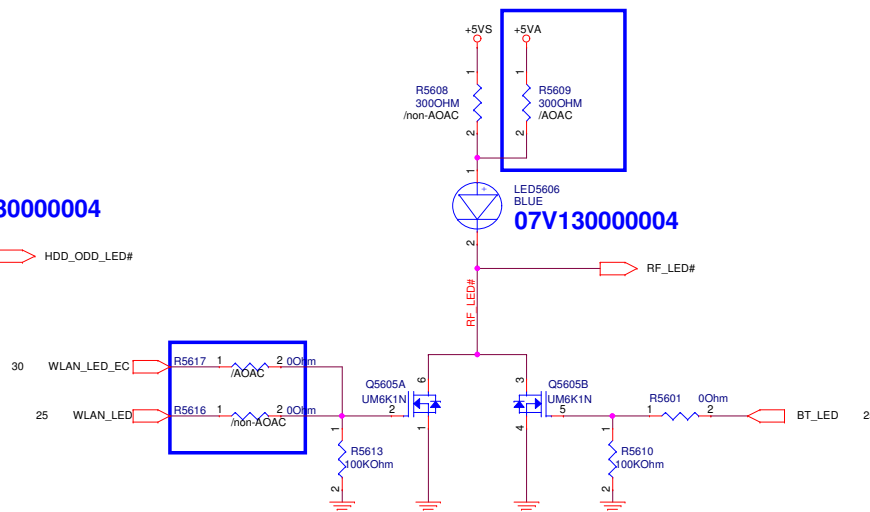
Battery



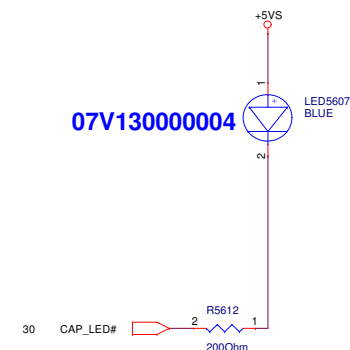
HDD/ODD



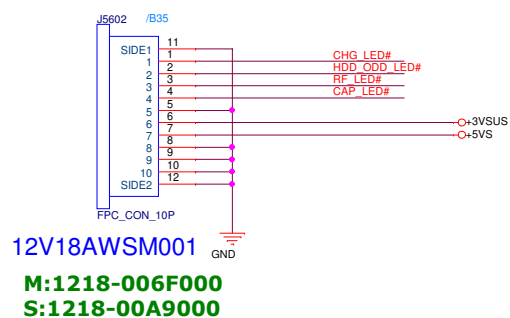
Connectivity (WLAN/BT/3G)



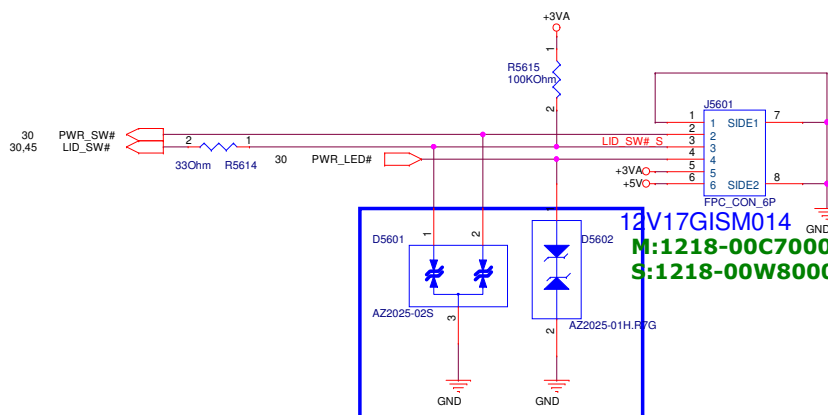
Caps Lock



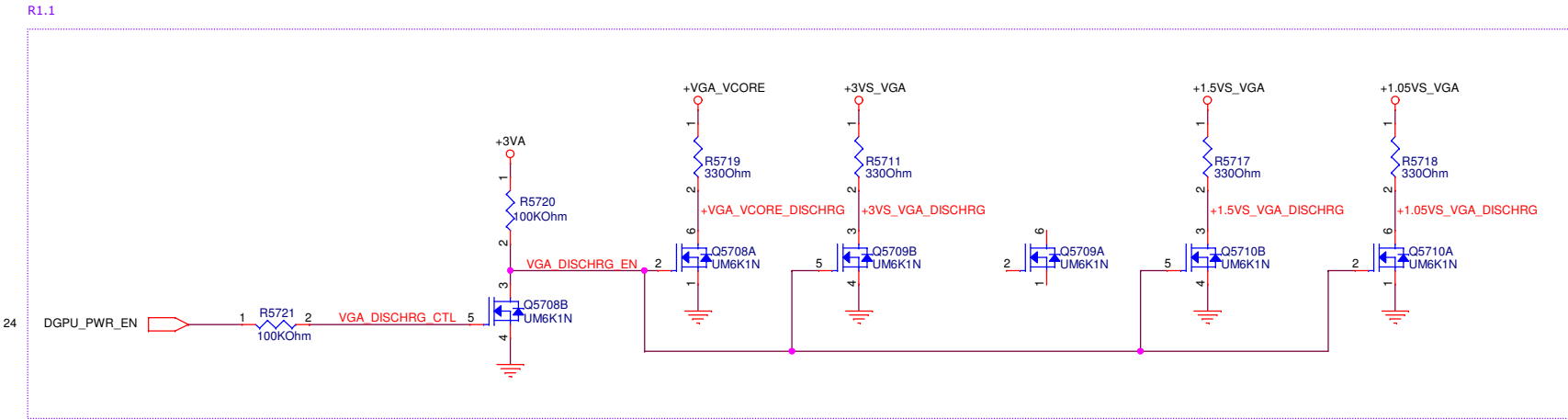
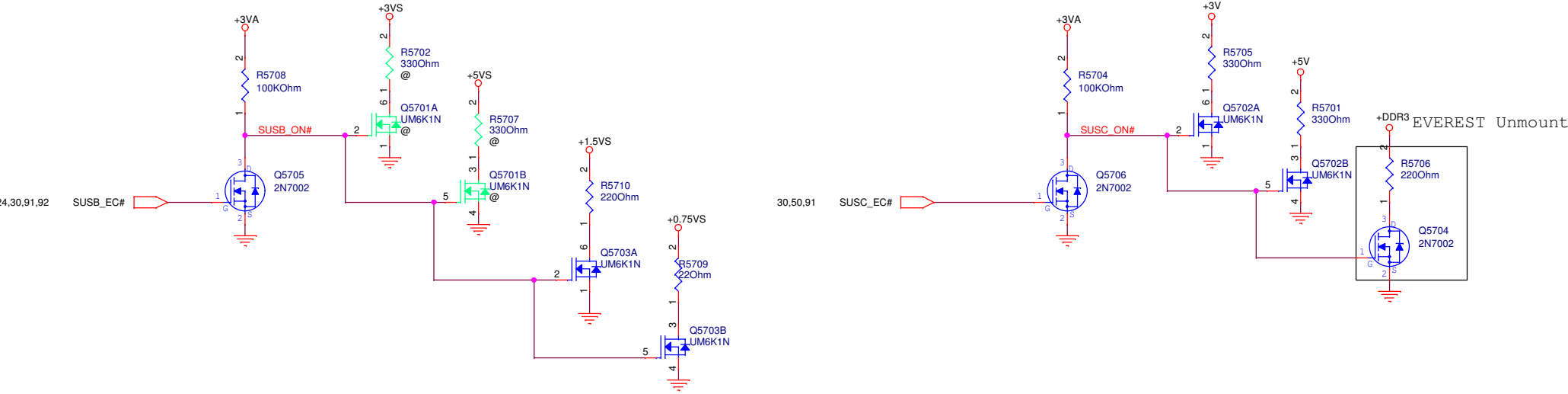
LED Board



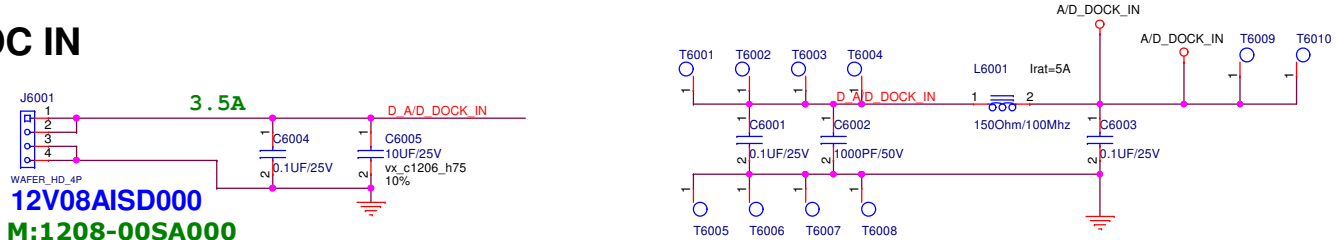
Power Switch Board Conn



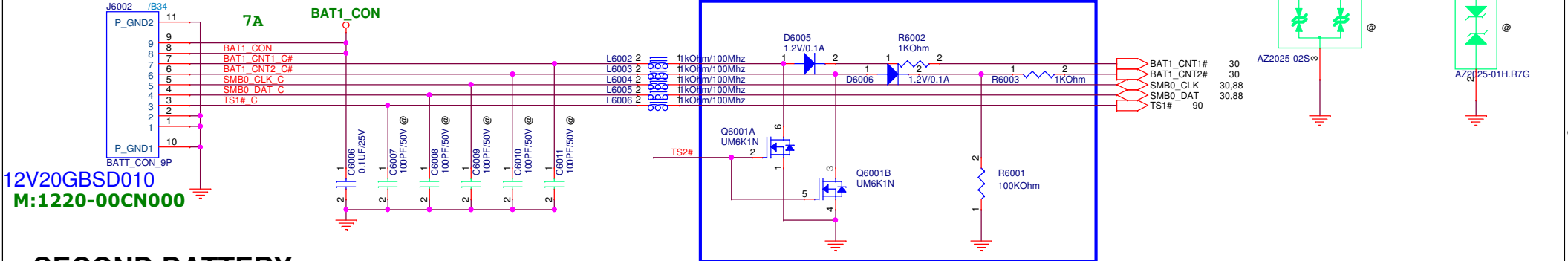
Discharge Circuit



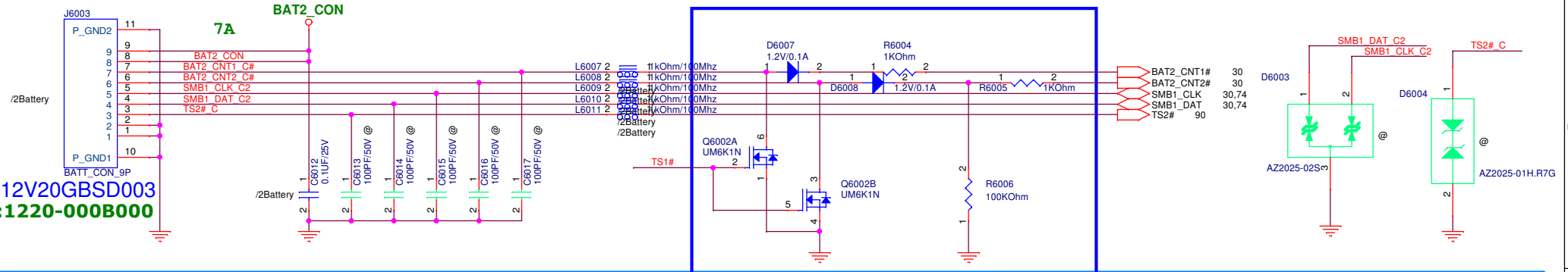
DC IN



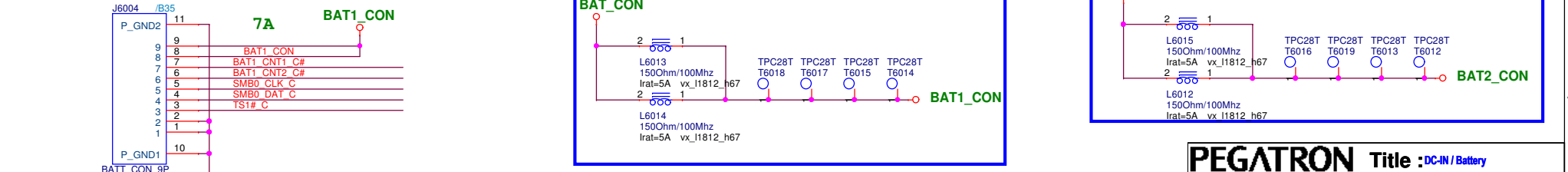
14" BATTERY
MAIN BATTERY



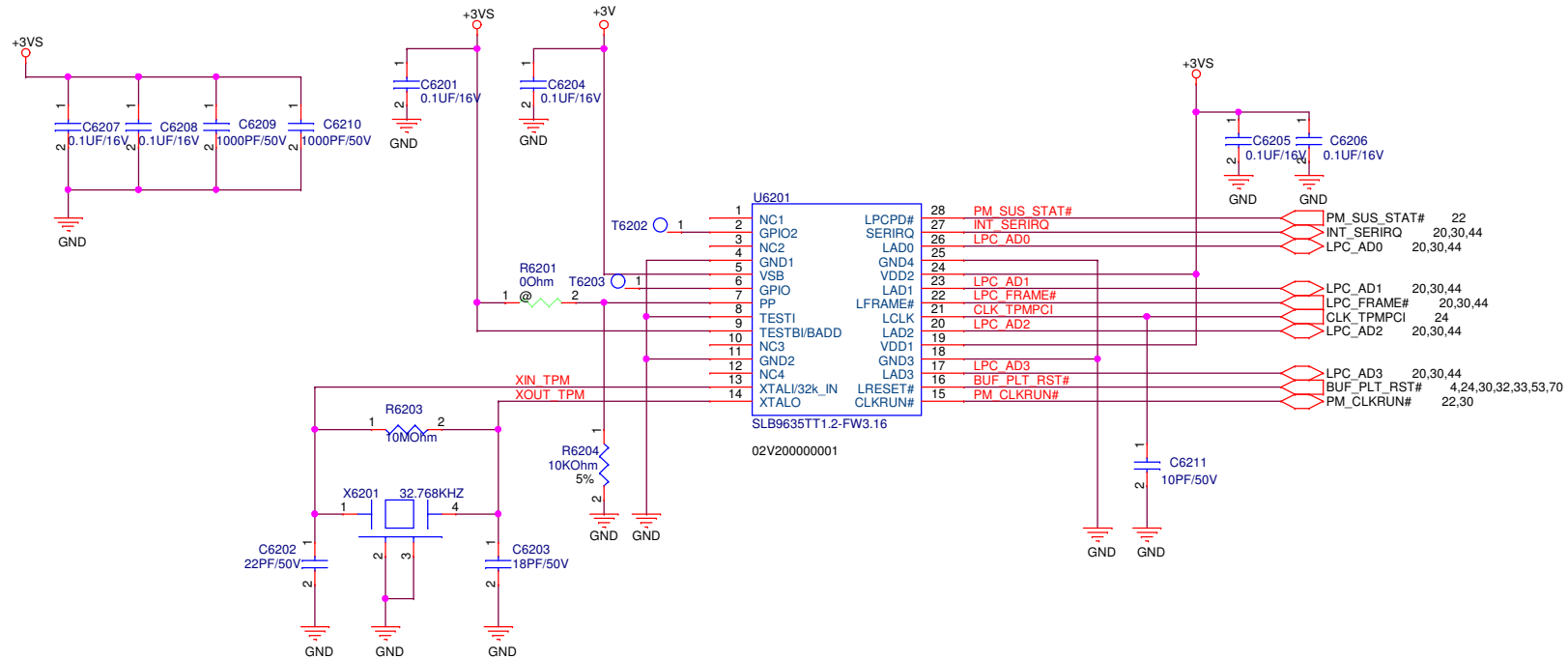
SECOND BATTERY



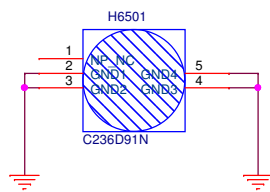
15" BATTERY



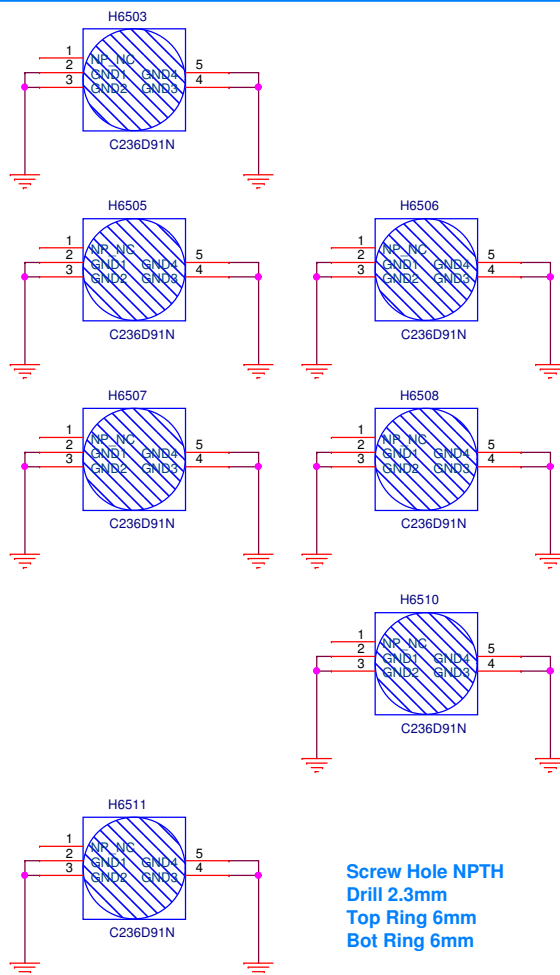
Infinion TPM Chip



PEGATRON		Title : TPM_****	
BG1VHW1		Engineer: Trunks Chen	
Size B	Project Name B34		Rev 2.1
Date: Wednesday, February 01, 2012		Sheet 62 of 98	

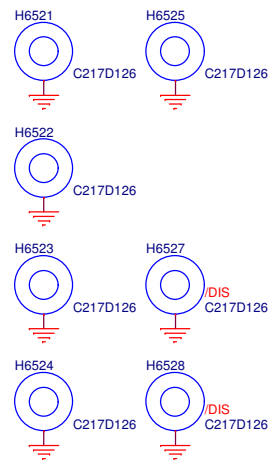


Screw Hole NPTH
Drill 2.3mm
Top Ring 7mm
Bot Ring 7mm



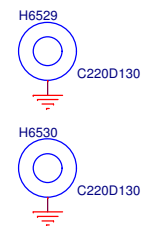
Screw Hole NPTH
Drill 2.3mm
Top Ring 6mm
Bot Ring 6mm

CPU & GPU & FAN

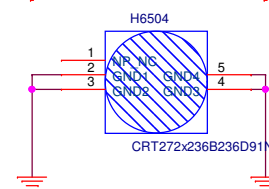
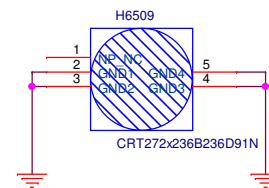
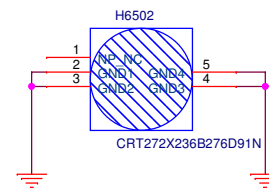
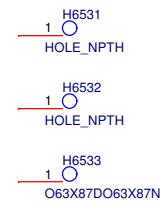
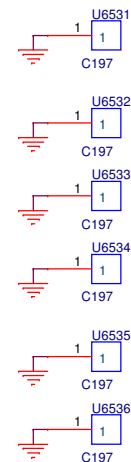


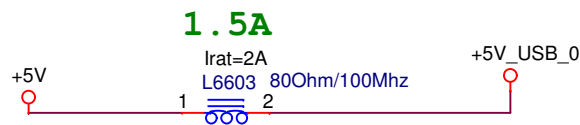
NUT
Drill 3.2mm(126)
Top Ring 5.5mm(217)
Bot Ring 5.5mm(217)

PCH

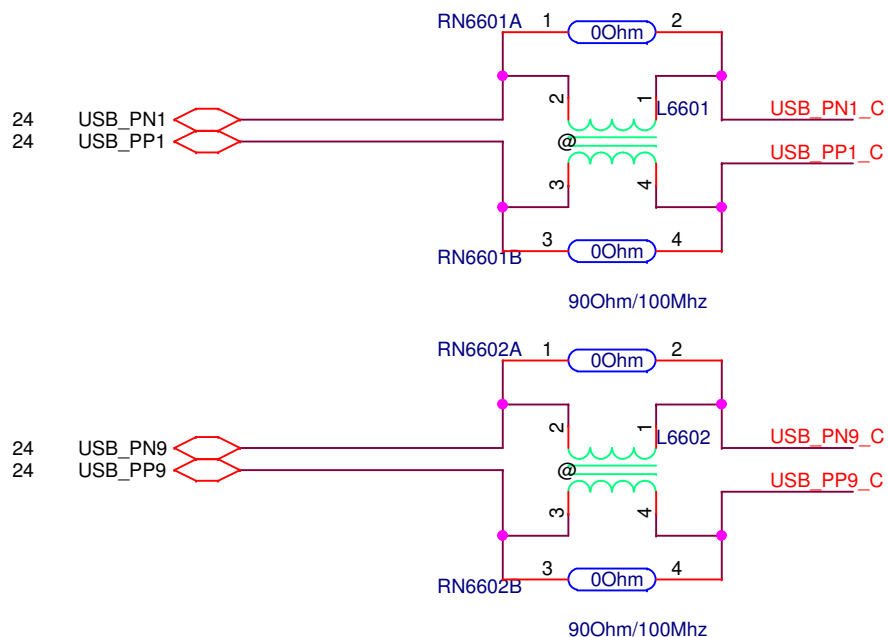
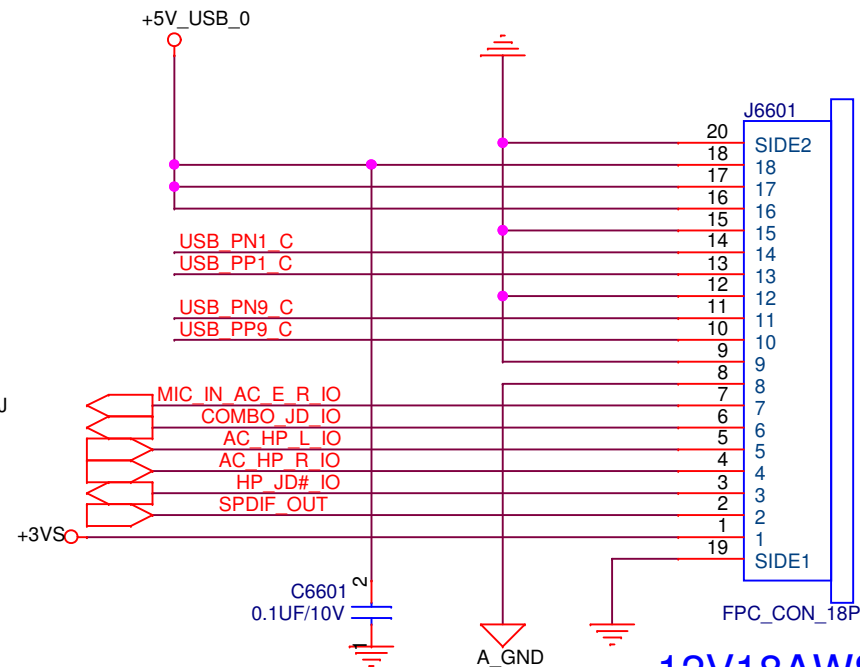


NUT H=4mm
Drill 3.3mm
Top Ring 5.5mm
Bot Ring 5.5mm



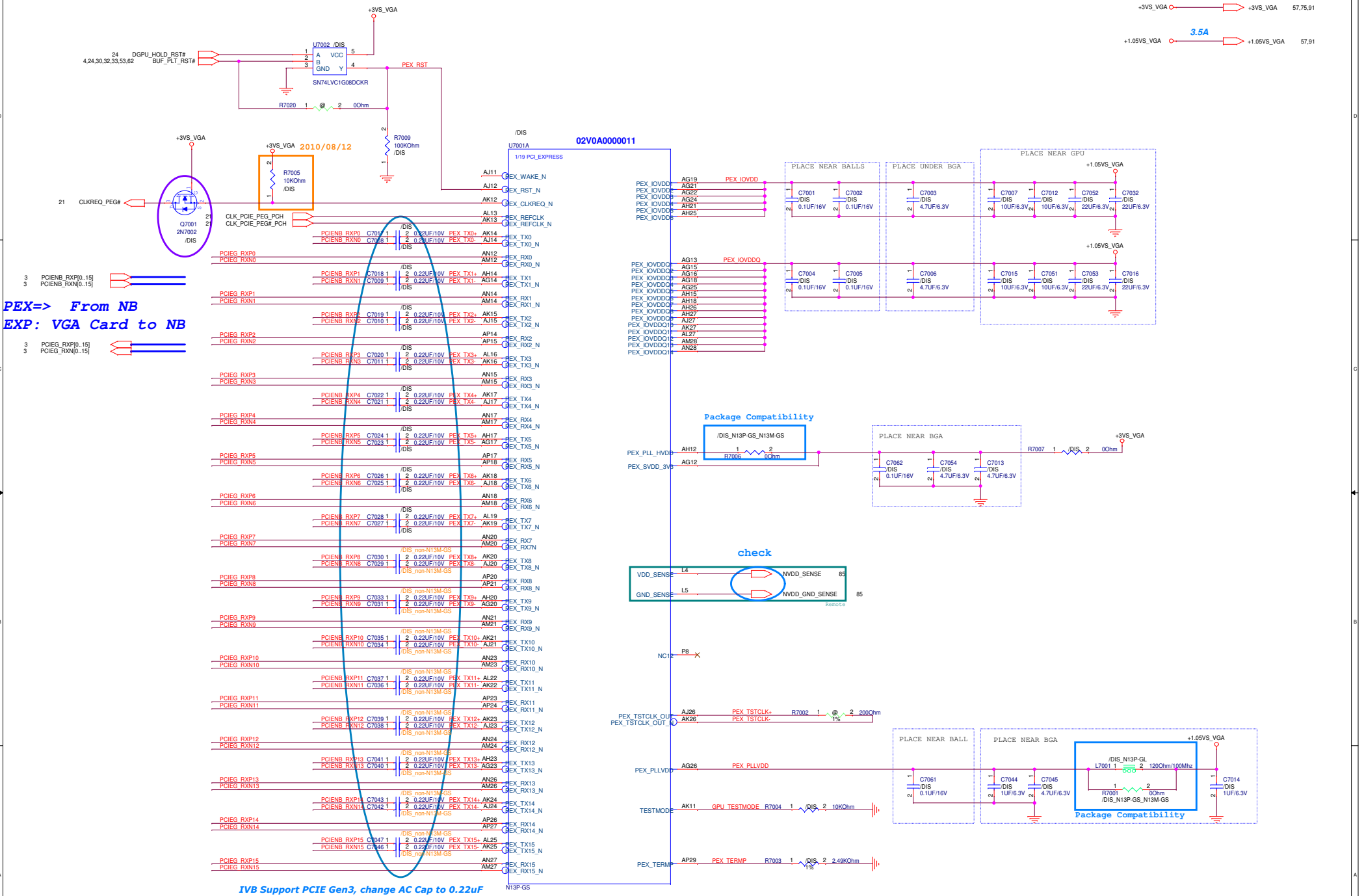


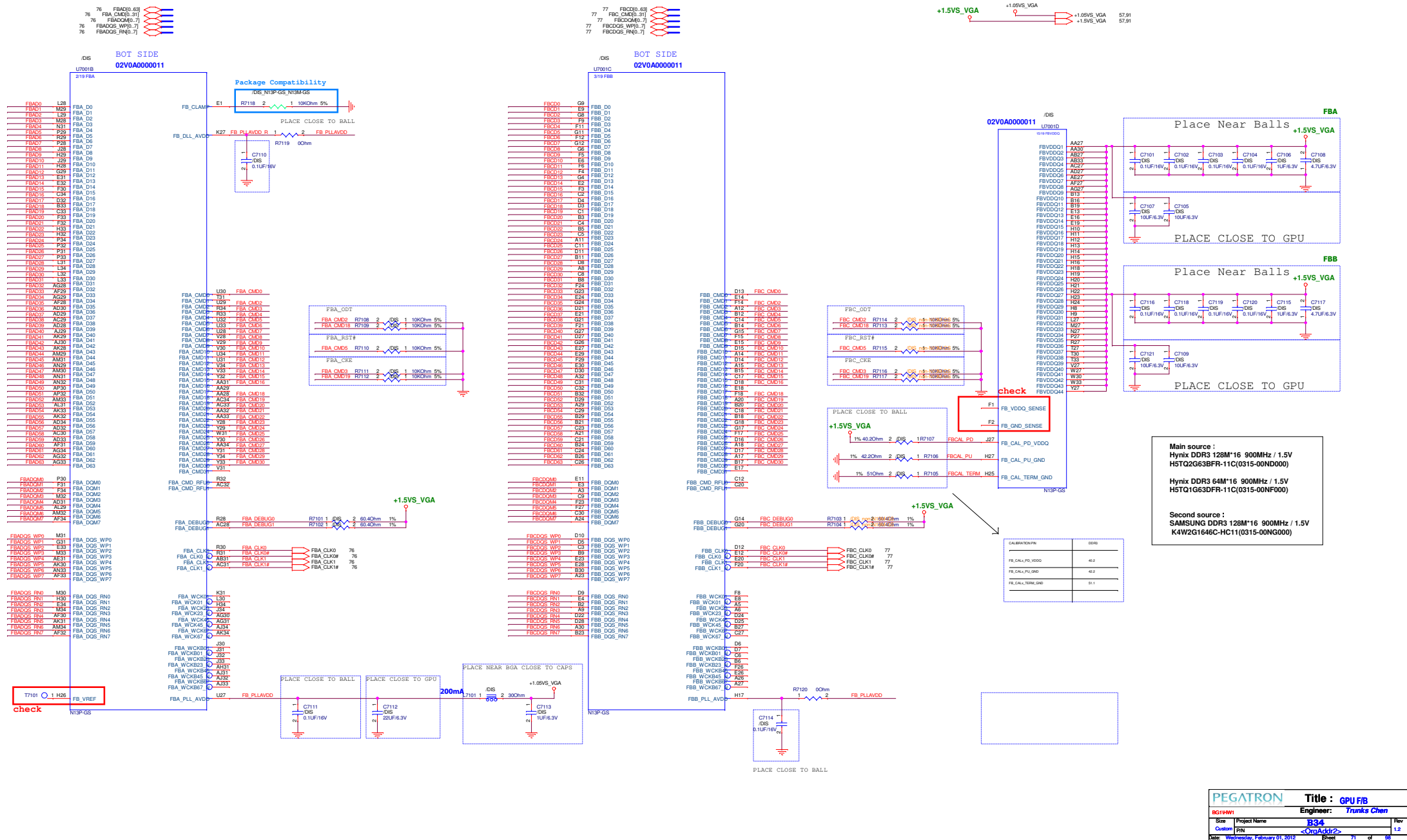
38 MIC_IN_AC_E_J
38 COMBO_JD
38 HP_JACK_L
38 HP_JACK_R
38 HP_JD#_M
38 SPDIF_OUT

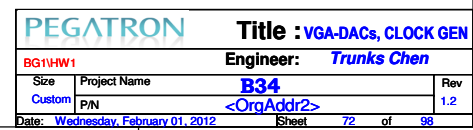
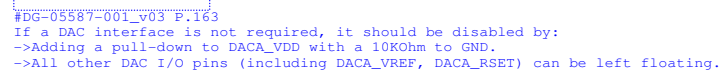


12V18AWSM008
M:1218-0162000
S:1218-0189000

PEGATRON		Title : IO_BOARD_CONN.	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Trunks Chen	
Size A	Project Name B34		Rev 1.0
Date: Wednesday, February 01, 2012		Sheet	66 of 99

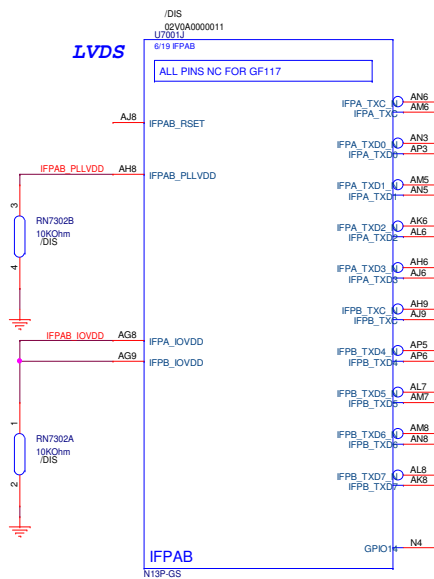




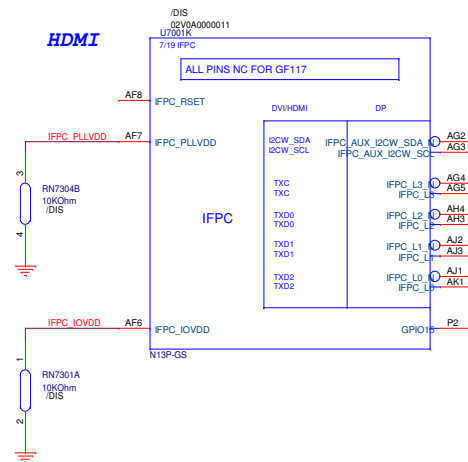


+3VS_VGA → +3VS_VGA 57,75,91
+1.05VS_VGA → +1.05VS_VGA 57,91

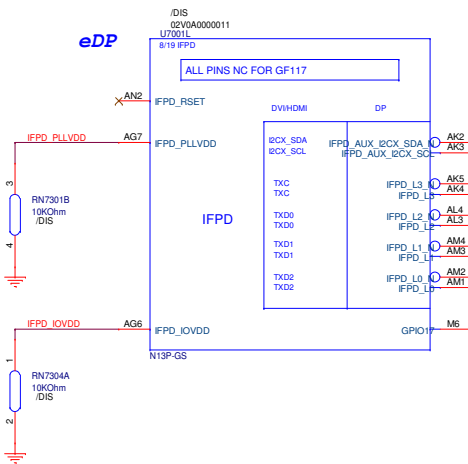
LVDS



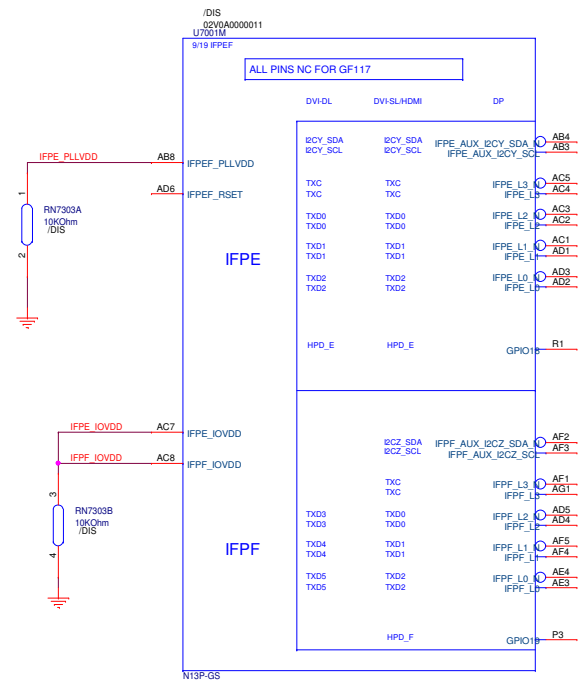
HDMI

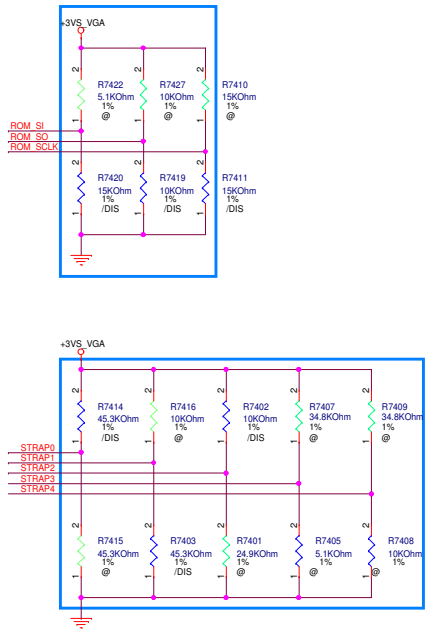
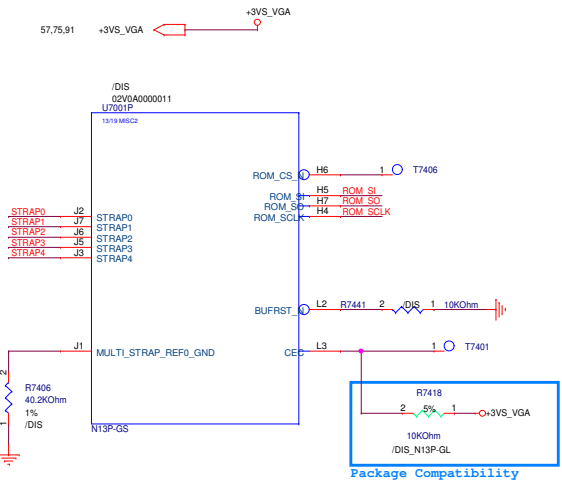


eDP



IFPE





STRAP0

```

USER[3:0]
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA +/-
0 0 0 1 XGA +/-
0 0 1 0 SXGA +/-
0 0 1 1 SXGA +/-
0 1 0 0 UXGA +/-
1 1 1 1 EDID N/A
  
```

STRAP1

```

3GIO_PAD_CFG_ADR[3:0]
3 2 1 0 PANEL
0 0 0 0 RESERVED
0 1 1 0 NOTEBOOK
.
1 1 1 1 RESERVED
  
```

STRAP2

```

LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]
  
```

STRAP3

```

LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED
  
```

STRAP4

```

LOGICAL BIT
0 DP_PLL_VDD33V
1 PCIE_MAX_SPEED
2 PCIE_SPEED_CHANGE_GEN3
3 RESERVED
  
```

ROM_SI RAMCONFIG

```

RAMCFG[3:0]
Rynix 64Mx16 -> ram_cfg = 0x2 -> pull down 15K
Samsung 64Mx16 -> ram_cfg = 0x3 -> pull down 20K
Rynix 128Mx16 -> ram_cfg = 0x6 -> pull down 35K
Samsung 128Mx16 -> ram_cfg = 0x7 -> pull down 45K
  
```

ROM_S0

```

LOGICAL BIT
3 FB[1]
2 FB[0]
1 SMB_ALT_ADDR
0 VGA_DEVICE
  
```

ROM_SCLK

```

LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDOR
1 PCI_DEVID[5]
0 PEK_PLL_EN_TERM
  
```

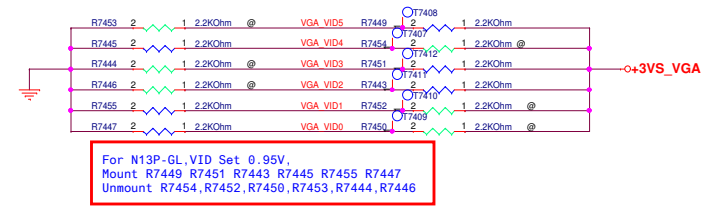
GB4-128

5K PU 1000 PD 0000
10K PU 1001 PD 0001
15K PU 1010 PD 0010
20K PU 1011 PD 0011
25K PU 1100 PD 0100
30K PU 1101 PD 0101
35K PU 1110 PD 0110
45K PU 1111 PD 0111

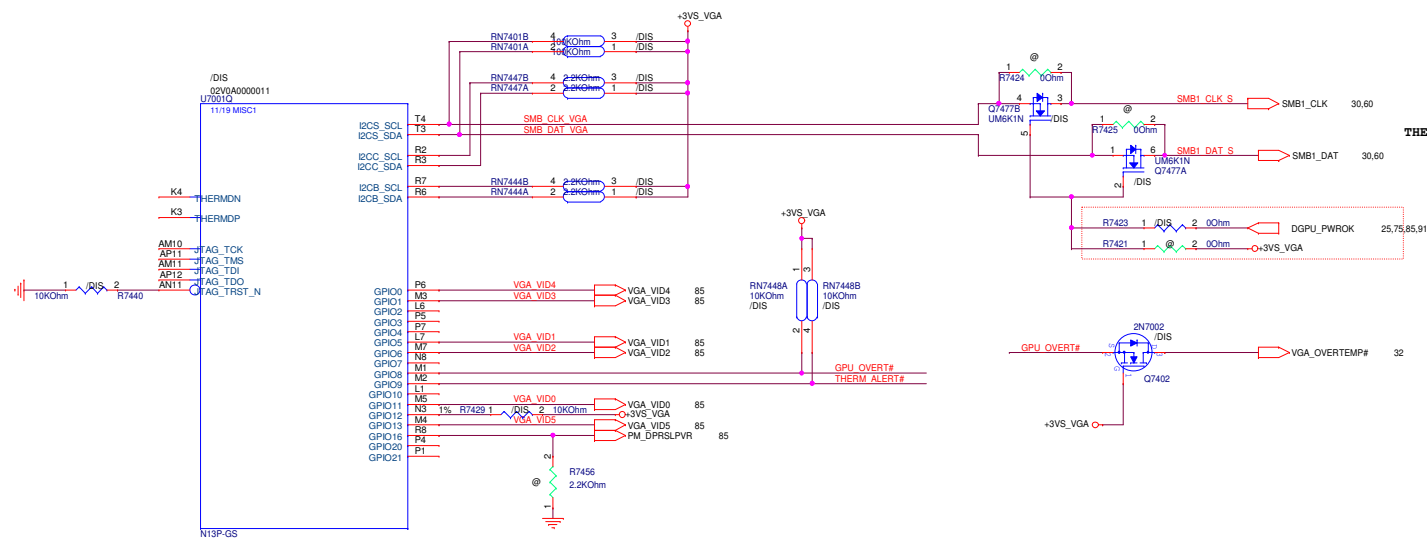
N13P-GL default NC --> reference DA-05691

N13P-GL - Strap1--> 07 --> reference DA-05691

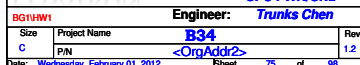
PCI_DEVID
N13P-GL --> 0X0DE9 - 1 0 0 1 --> pull up 10K



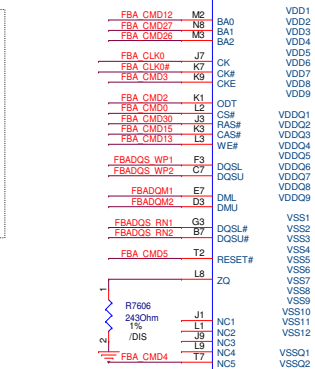
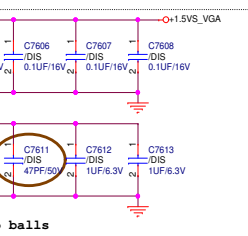
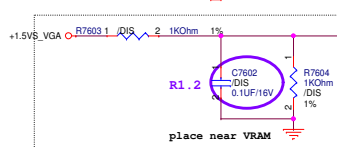
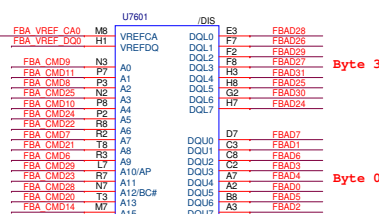
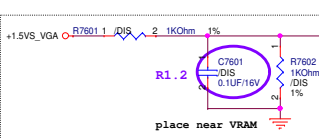
GPIO USAGE			
GPIO	I/O	ACTIVE	USAGE
0	OUT	N/A	GPU_VID4
1	OUT	N/A	GPU_VID3
2	OUT	HIGH	LCD_BL_PWM_VGA
3	OUT	HIGH	LCD_VCC
4	OUT	HIGH	LCD_BLEN
5	OUT	HIGH	GPU_VID1
6	OUT	HIGH	GPU_VID2
7	OUT	HIGH	3D Vision
8	IN/OUT	LOW	OVERT
9	IN/OUT	LOW	ALERT
10	OUT	HIGH	MEM_VREF_CTL
11	OUT	HIGH	GPU_VID0
12	IN	N/A	PWR_LEVEL
13	OUT	LOW	GPU_VID5
14	IN	HIGH	HPD_AB
15	IN	N/A	HPD_C
16	OUT	N/A	MEM_VDD_CTL
17	IN	N/A	HPD_D
18	IN	N/A	HPD_E
19	IN	N/A	HPD_F
20			RESERVED
21			RESERVED



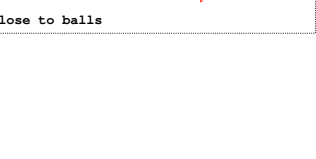
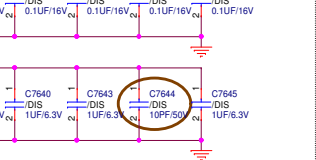
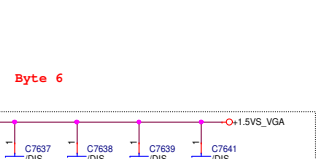
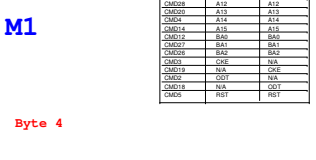
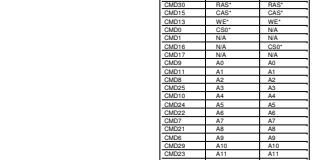
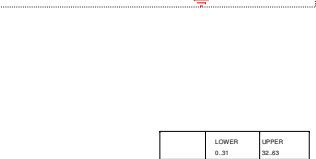
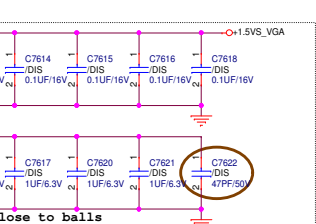
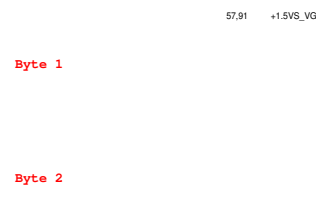
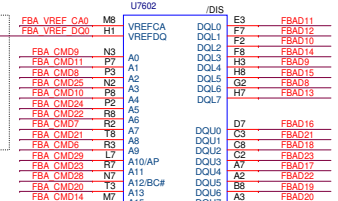
GPU_VID	VID1	VID0	+VGA_VCORE
Low	0	0	
Med	0	1	
High	1	0	



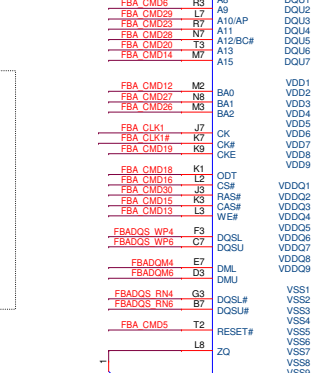
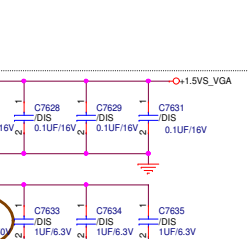
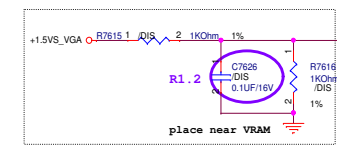
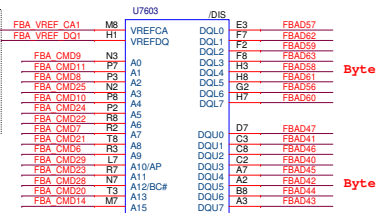
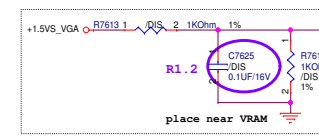
VRAM CH A



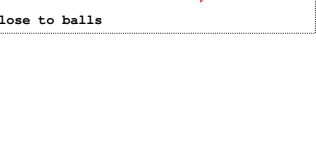
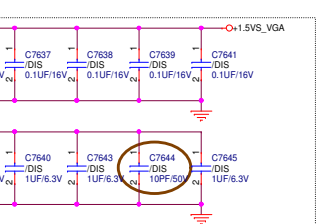
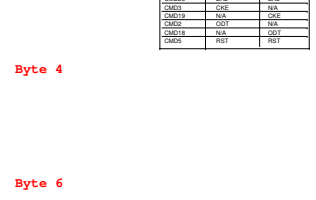
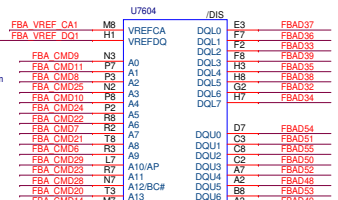
BOT SIDE --- M0



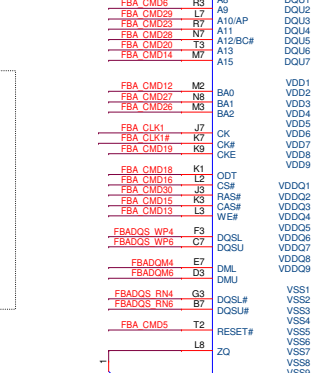
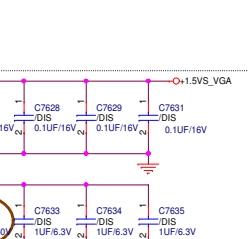
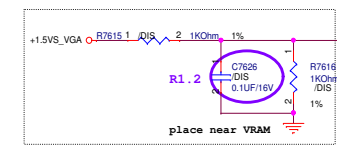
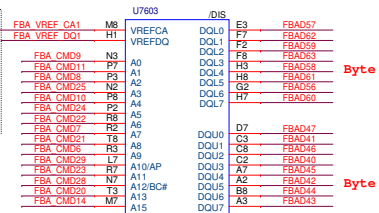
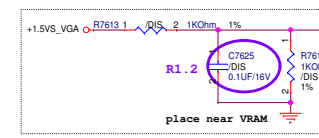
TOP SIDE --- M3



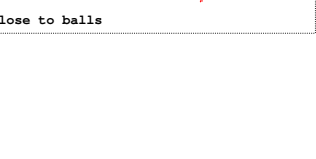
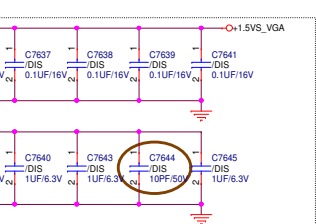
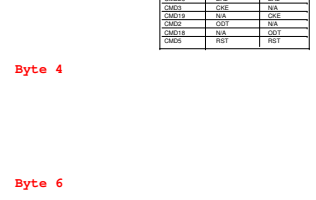
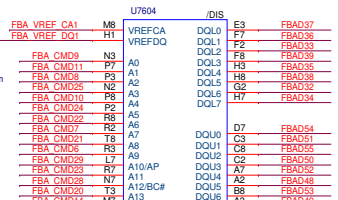
BOT SIDE --- M1



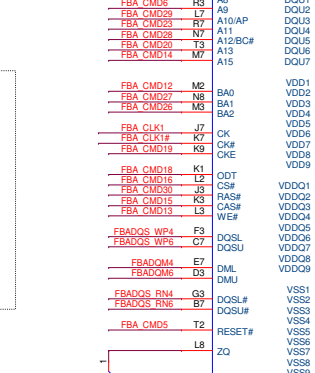
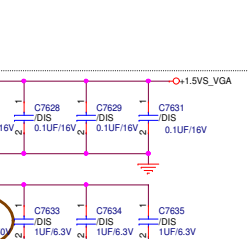
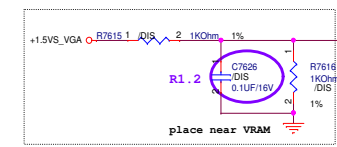
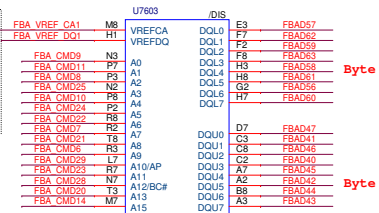
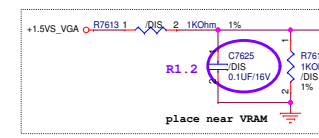
TOP SIDE --- M2



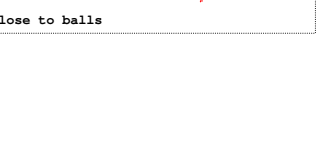
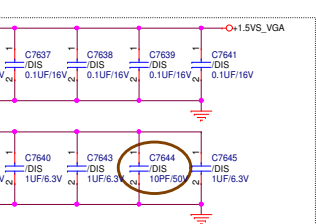
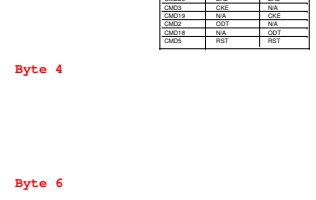
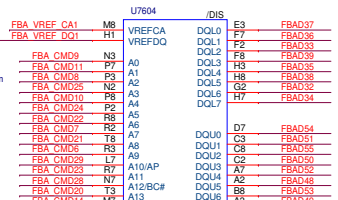
BOT SIDE --- M0



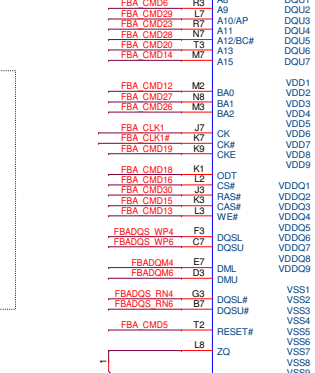
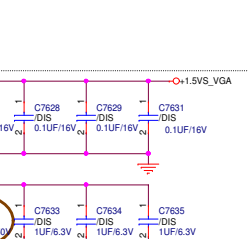
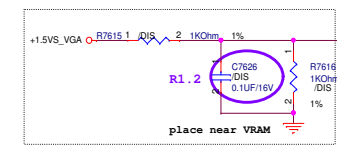
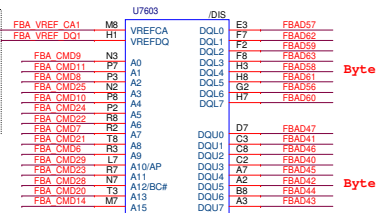
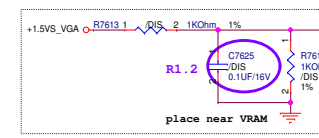
TOP SIDE --- M3



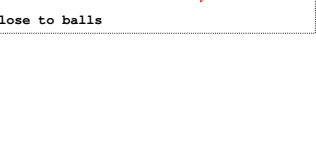
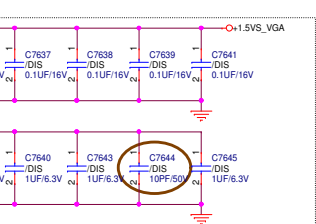
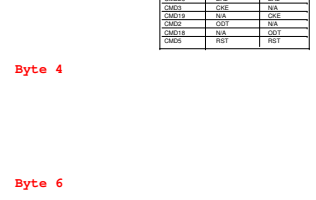
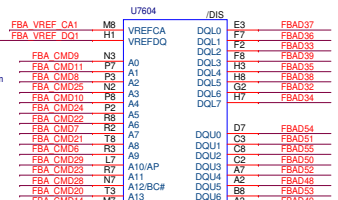
BOT SIDE --- M1



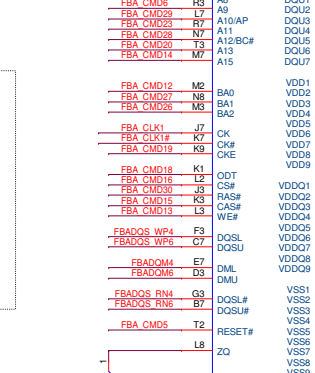
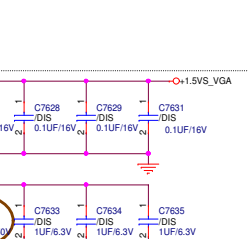
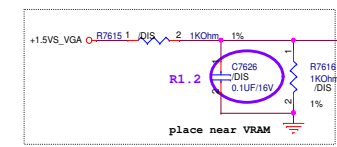
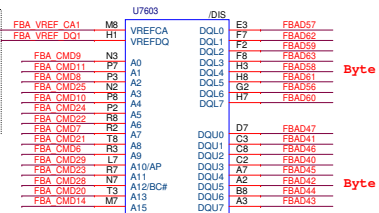
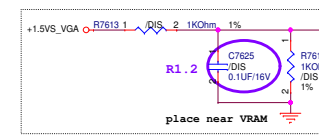
TOP SIDE --- M2



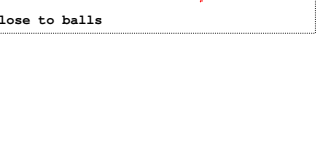
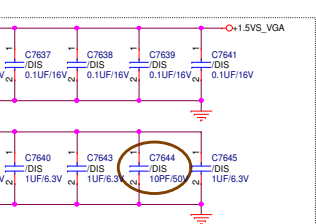
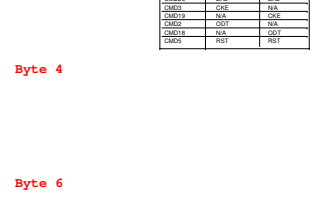
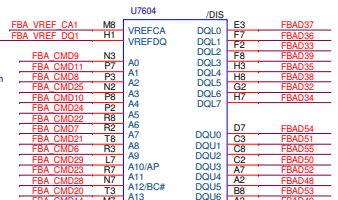
BOT SIDE --- M0



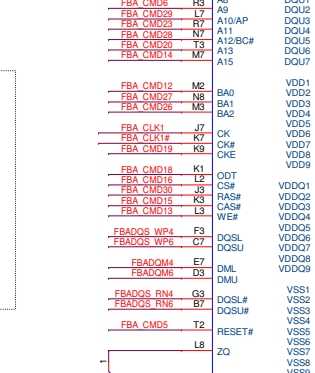
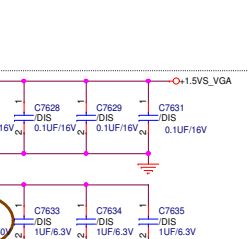
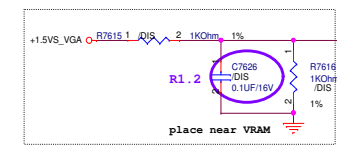
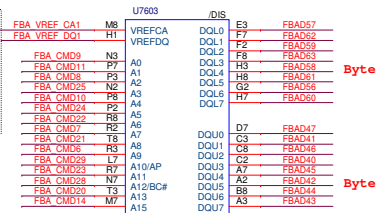
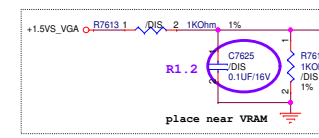
TOP SIDE --- M3



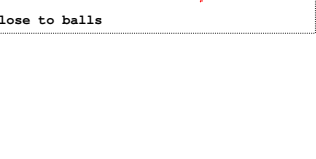
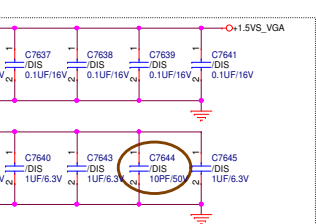
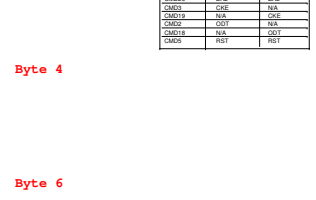
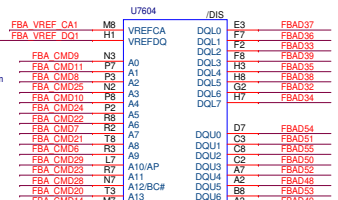
BOT SIDE --- M1



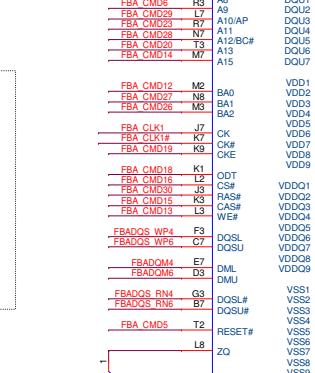
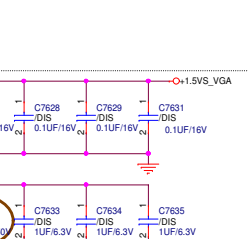
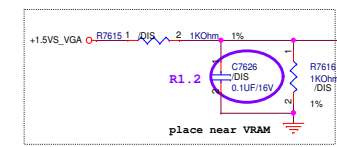
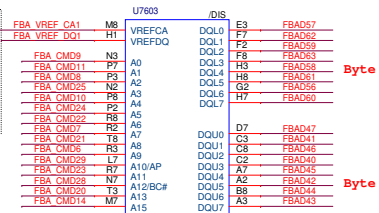
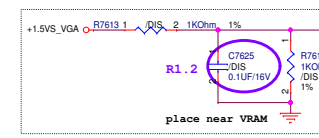
TOP SIDE --- M2



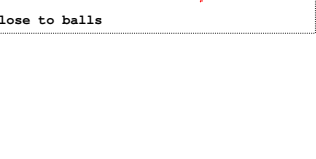
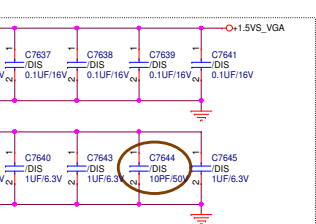
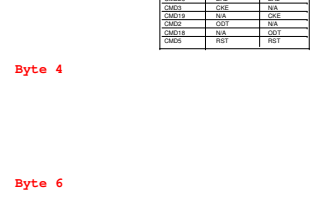
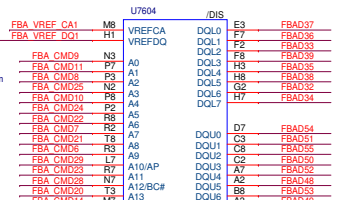
BOT SIDE --- M0



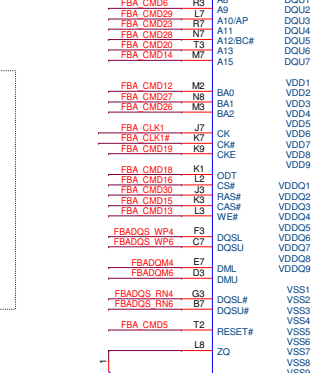
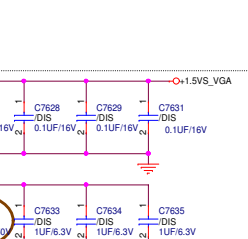
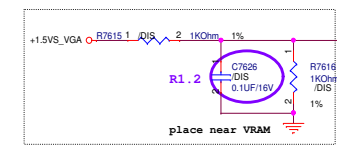
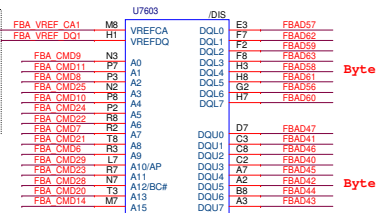
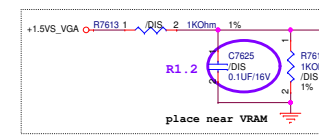
TOP SIDE --- M3



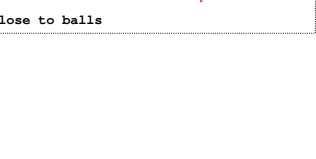
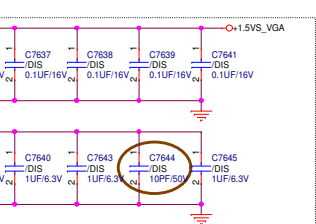
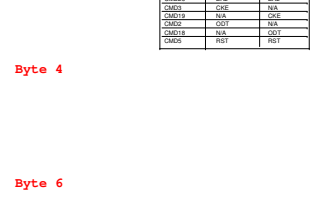
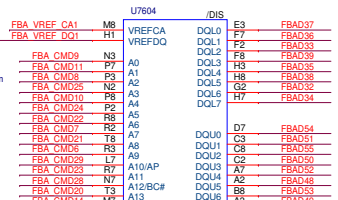
BOT SIDE --- M1



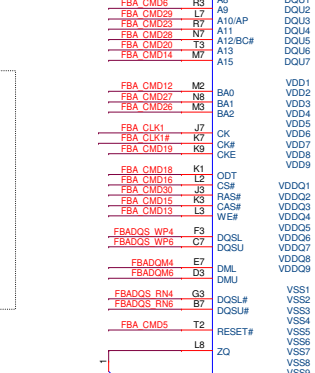
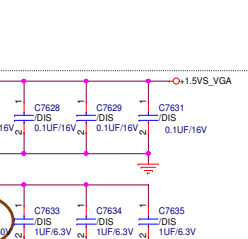
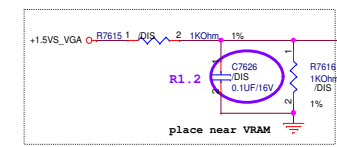
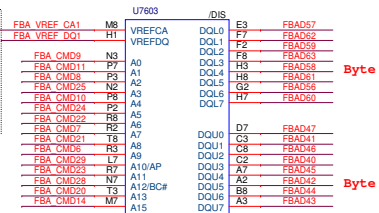
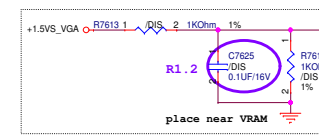
TOP SIDE --- M2



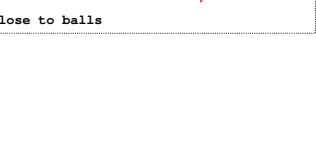
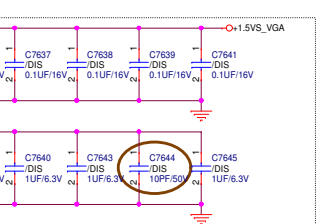
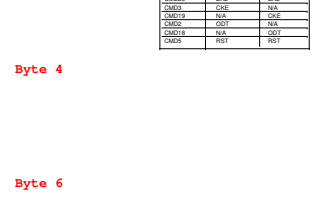
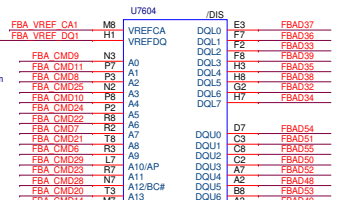
BOT SIDE --- M0



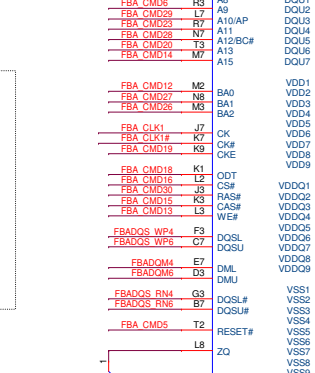
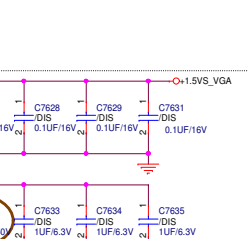
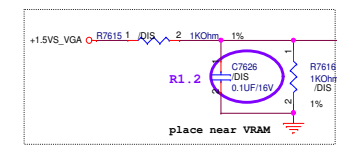
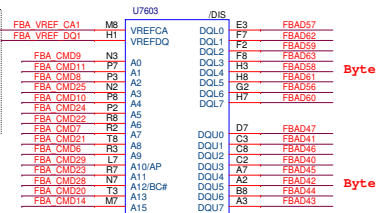
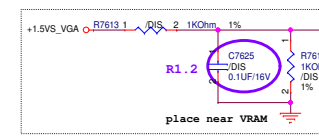
TOP SIDE --- M3



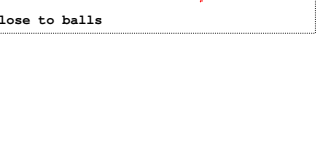
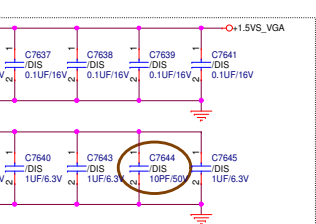
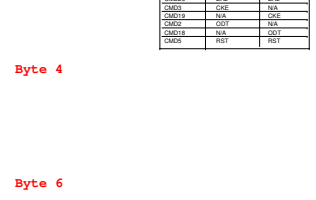
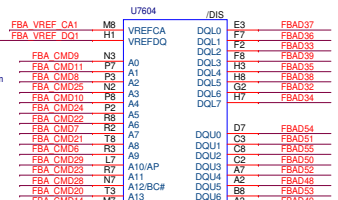
BOT SIDE --- M1



TOP SIDE --- M2



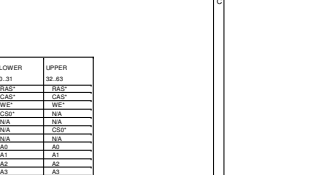
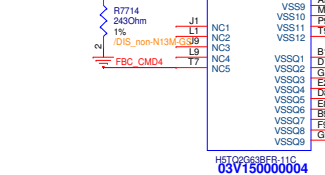
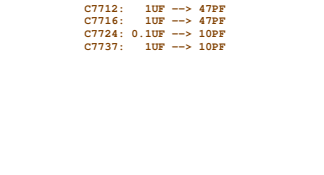
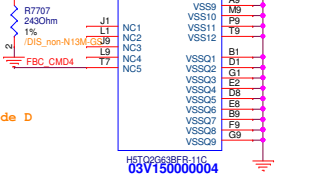
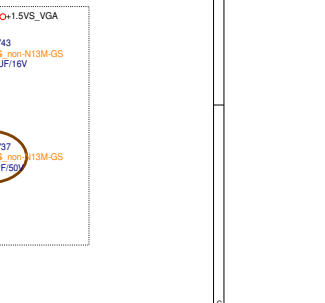
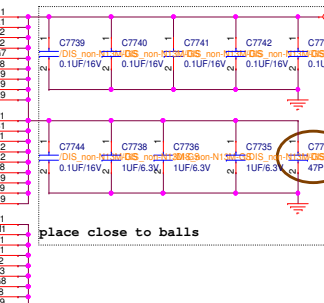
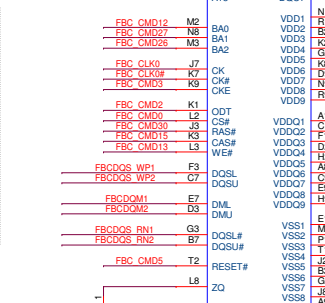
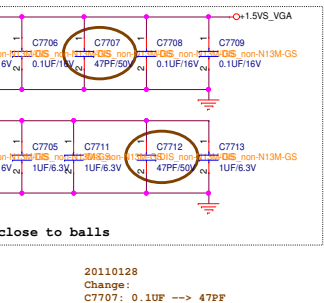
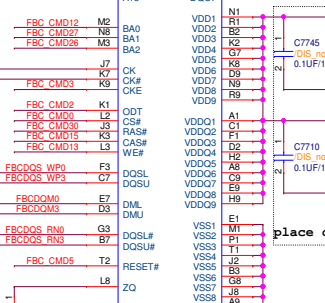
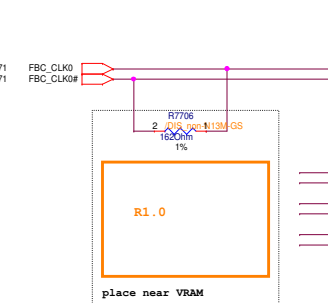
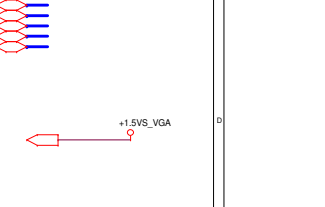
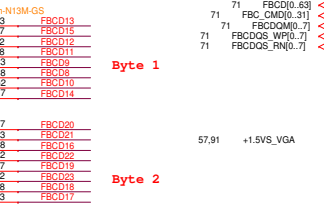
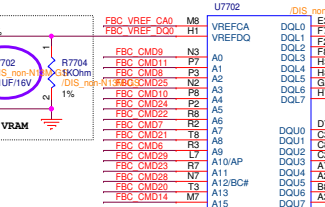
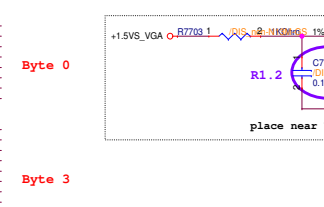
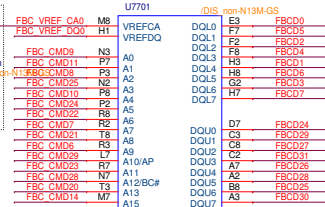
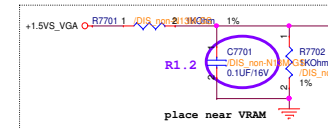
BOT SIDE --- M0



VRAM CH C

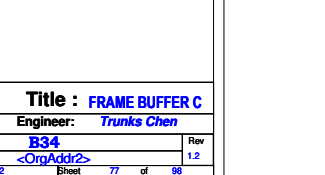
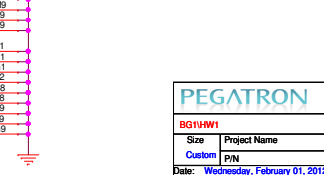
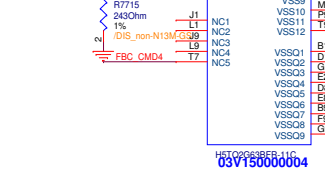
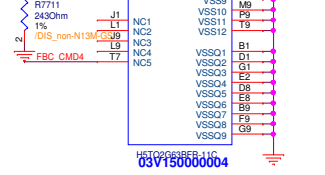
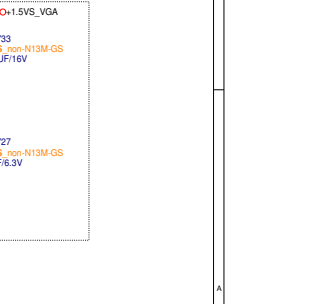
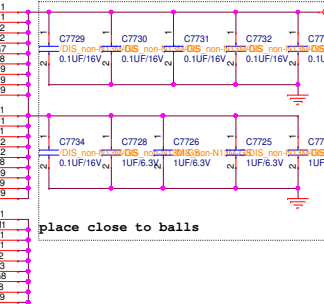
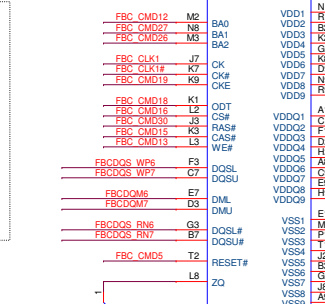
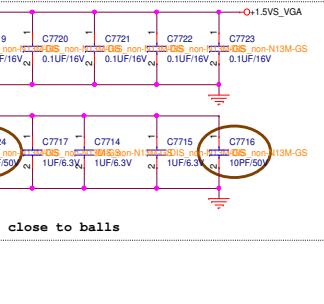
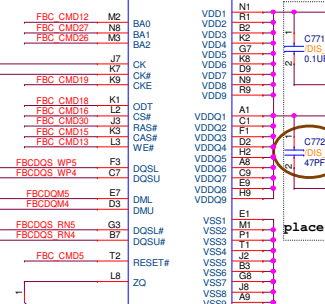
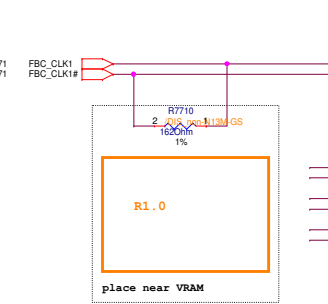
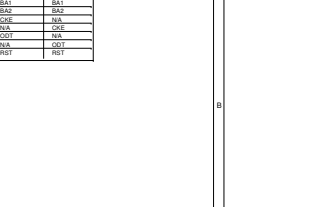
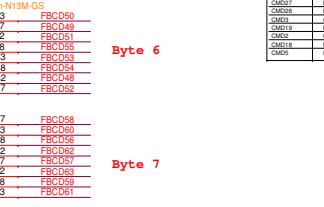
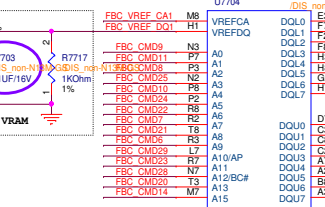
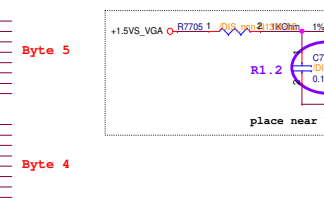
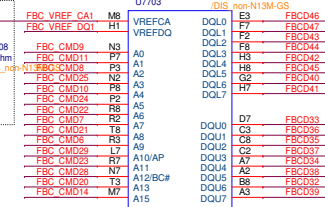
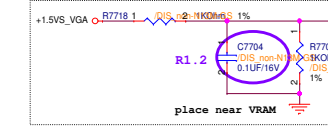
TOP SIDE --- M2

BOT SIDE --- M0



TOP SIDE --- M3

BOT SIDE --- M1






R1.0
delete Ventura.

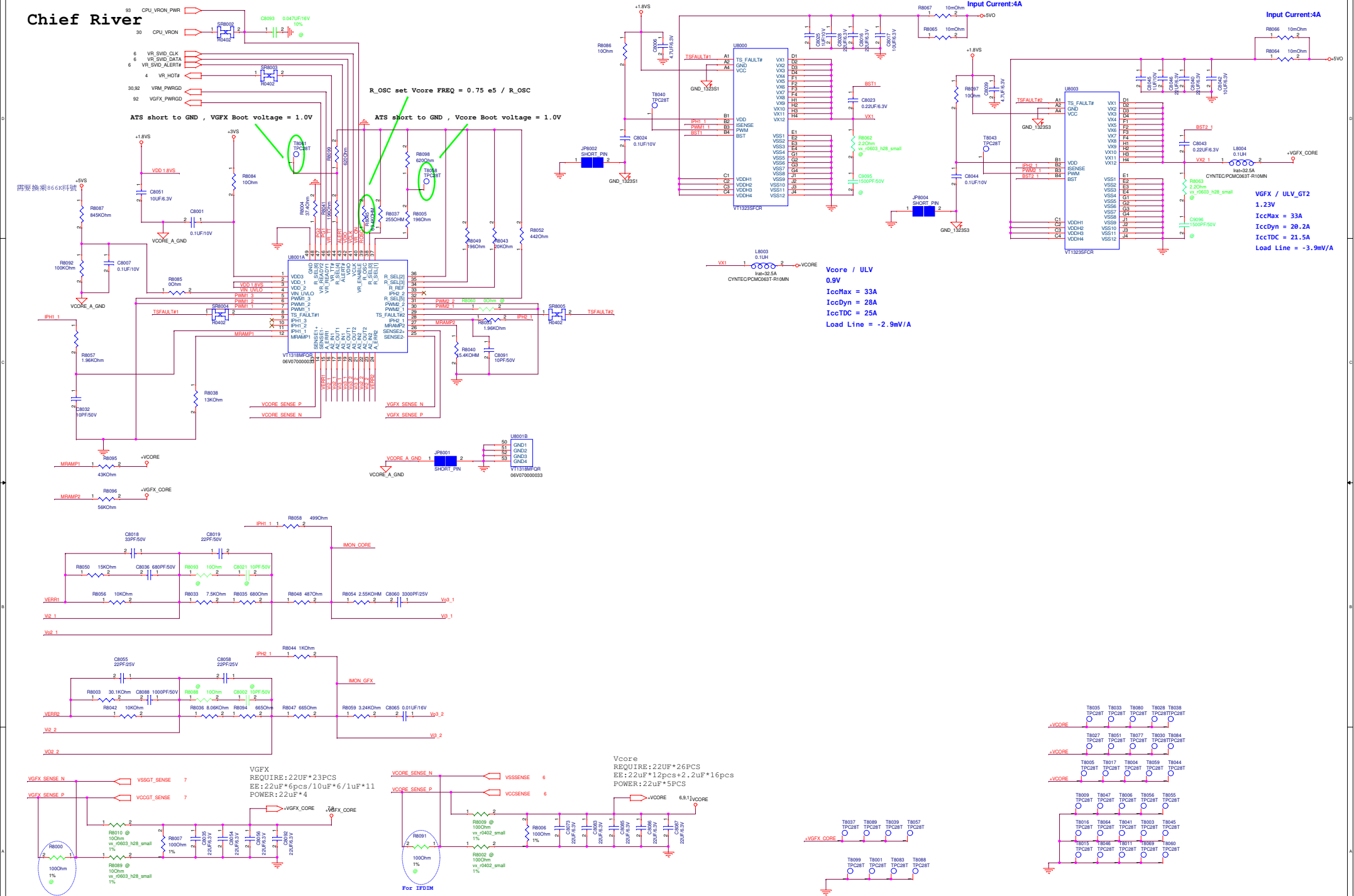
PEGATRON		Title :VGA_VENTURA_INA219	
PEGATRON COMPUTER INC		Engineer: <i>Trunks Chen</i>	
Size B	Project Name P/N	B34 <OrgAddr2>	Rev 1.2
Date: <i>Wednesday, February 01, 2012</i>		Sheet 78 of 98	

R1.0

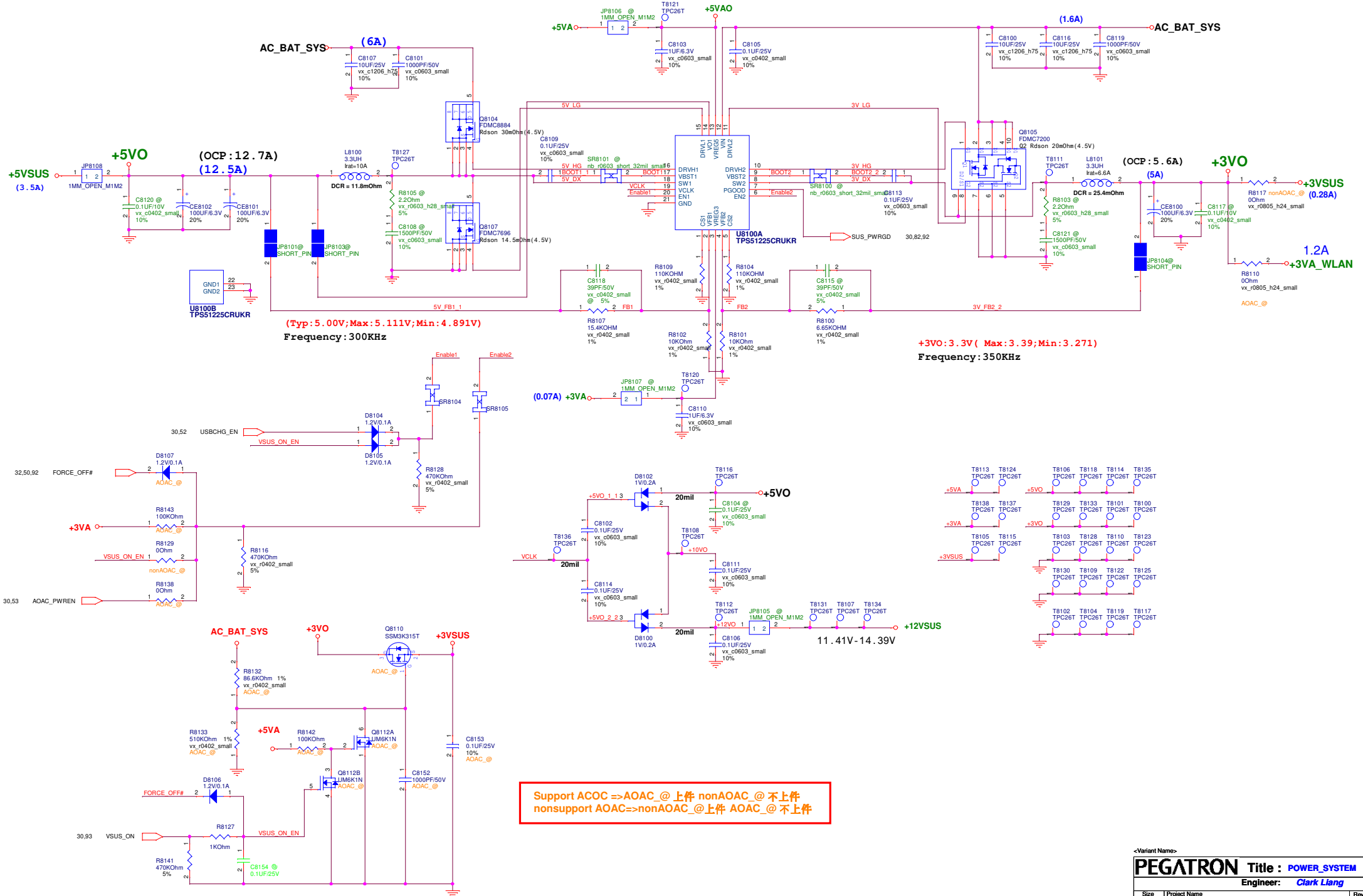
delete GB3-128 additional schematic.

		Title : ADDITIOAL	
BG1\HW1		Engineer: <i>Trunks Chen</i>	
Size	Project Name	Rev	
A	P/N	B34	1.2
Date: Wednesday, February 01, 2012		Sheet 79 of 98	

Chief Riv



+5VO & +3VO POWER SUPPLY



<Variant Name>

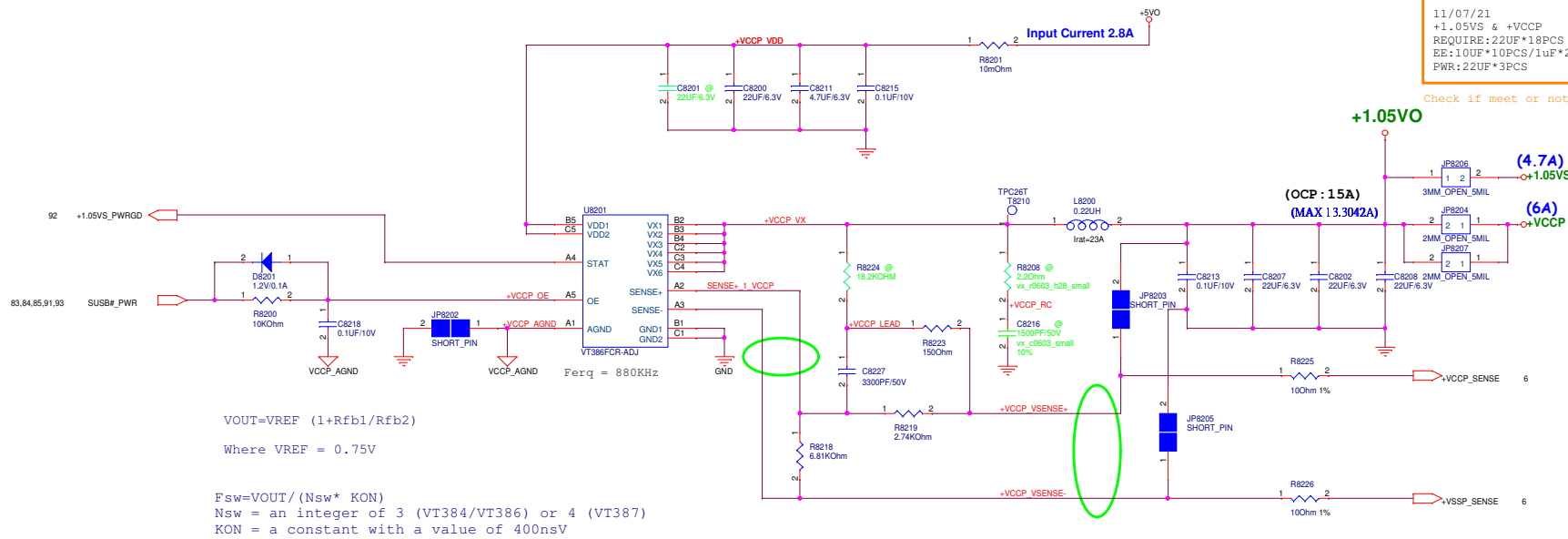
PEGATRON Title : **POWER_SYSTEM**

Engineer: **Clark Liang**

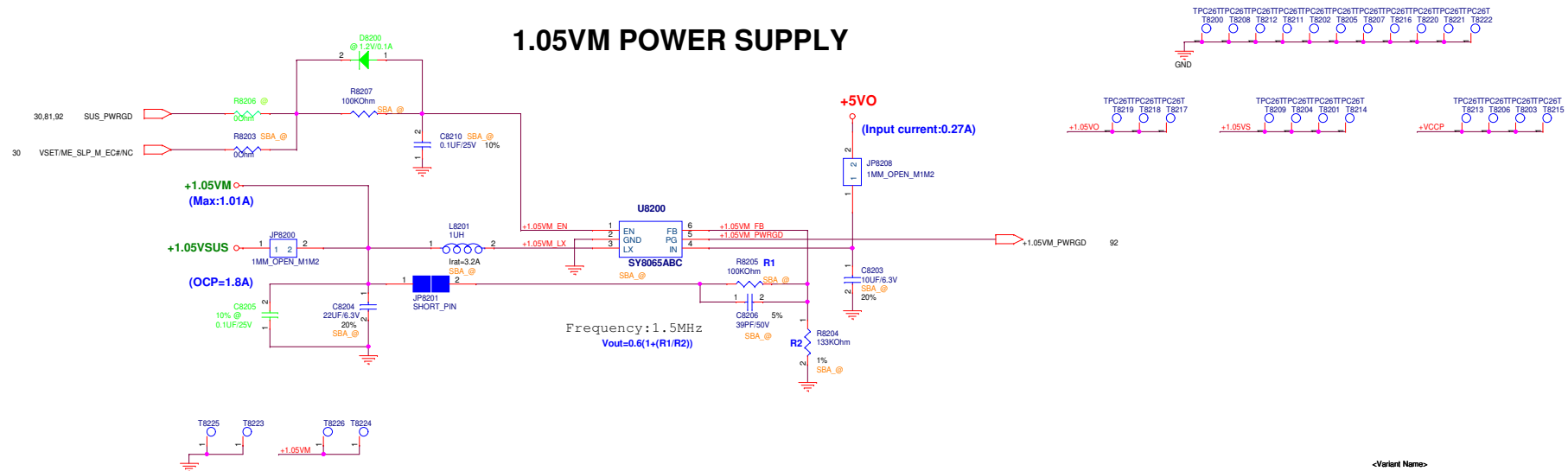
Size Project Name
Custom **U14** Rev 1.0

Date: Wednesday, February 01, 2012 Sheet 81 of 94

+1.05VO POWER SUPPLY



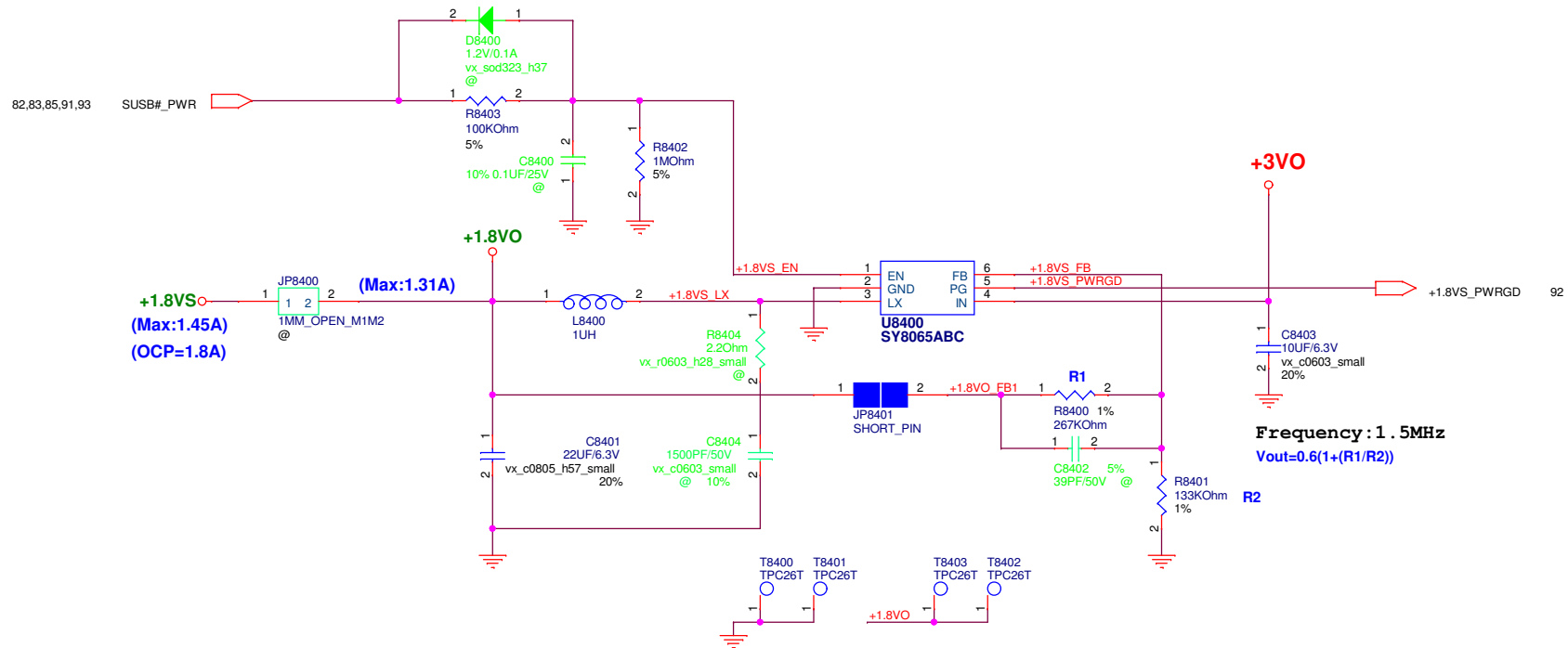
1.05VM POWER SUPPLY



11/07/21
+1.5VO
REQUIRE:22UF*6PCS
EE:10UF*8PCS/1uF*10PCS
PWR:22UF*3PCS

[illegible]

+1.8VS POWER SUPPLY



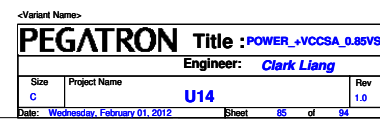
<Variant Name>

PEGATRON Title : **POWER_+1.8VS**

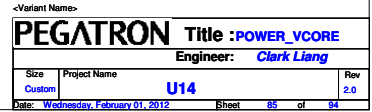
Engineer: **Clark Liang**

Size Custom	Project Name U14	Rev 1.0
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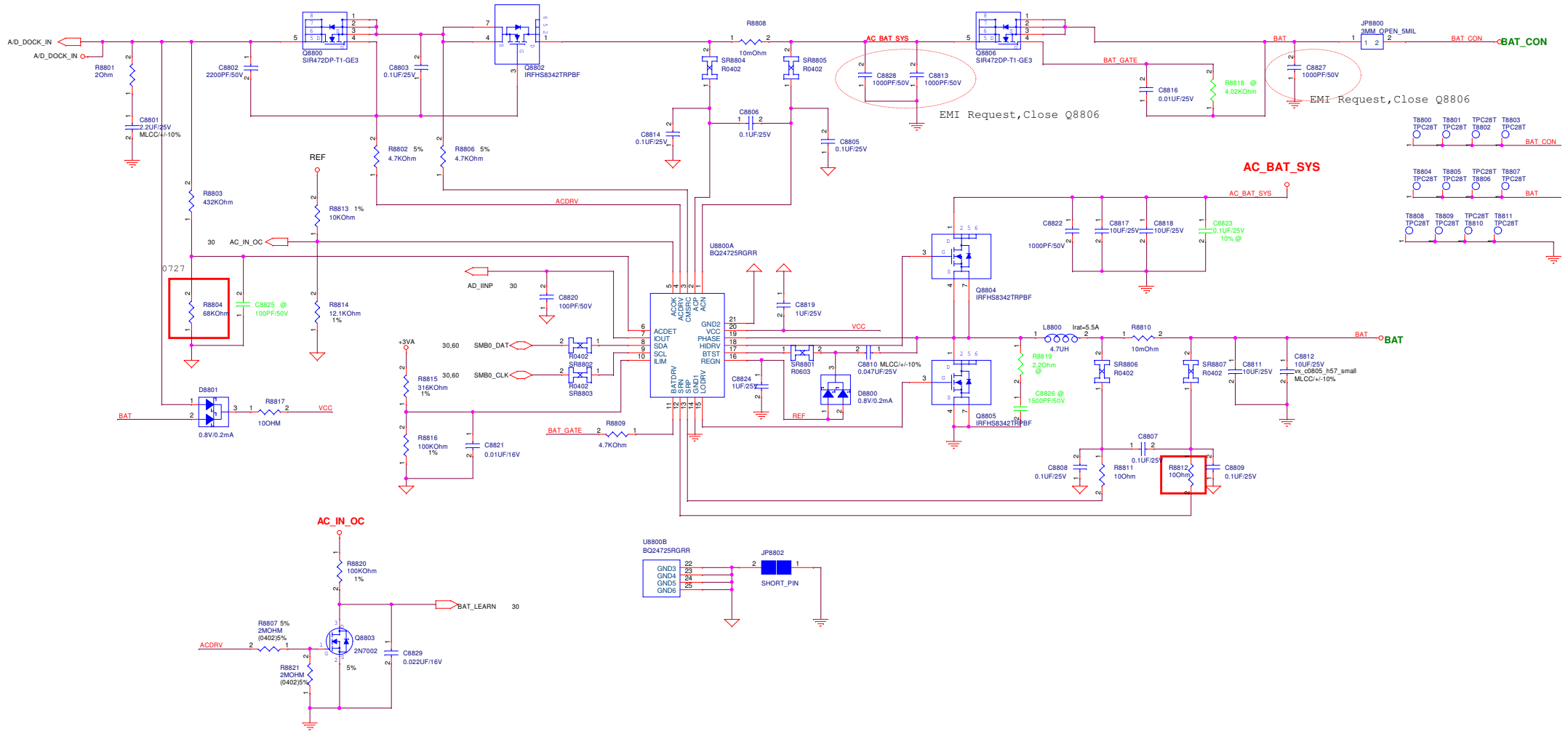
Date: Wednesday, February 01, 2012 Sheet 84 of 94



PM_DPRSPLVR	MODE
L	2 Phase CCM
H	2 Phase DCM



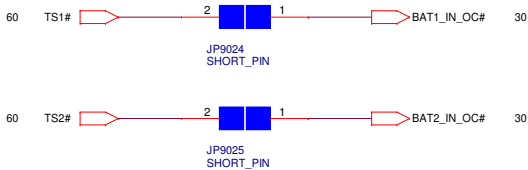
BATTERY CHARGER



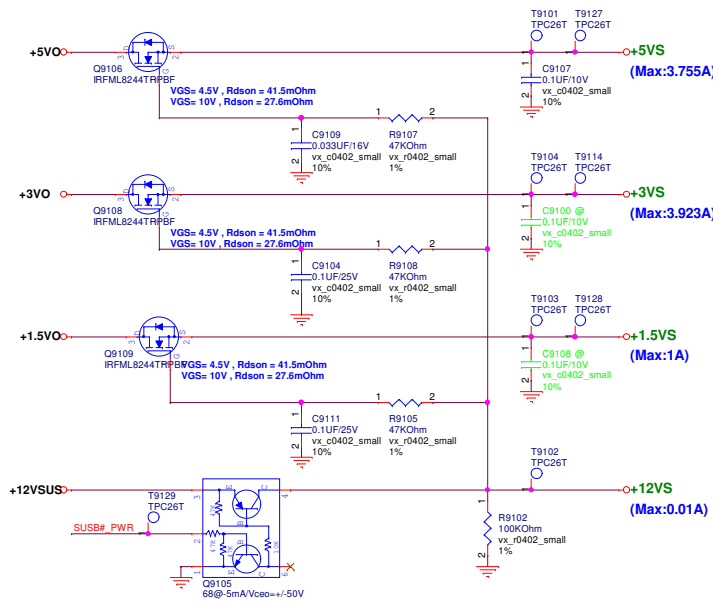
<Variant Name>

PEGATRON Title :POWER_CHARGER		
Engineer: Clark Liang		
Size	Project Name	Rev
Custom	U14	1.0
Date: Wednesday, February 01, 2012 Sheet 88 of 94		

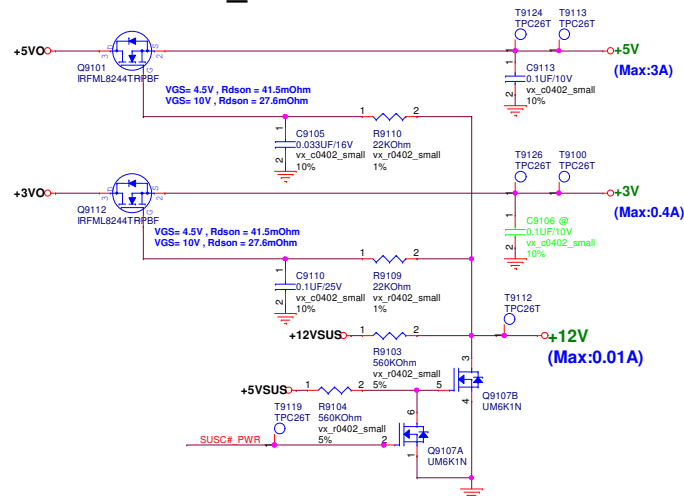
BATTERY IN DETECT



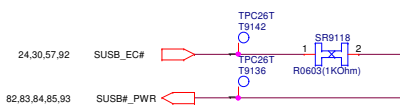
SUSB#_PWR POWER



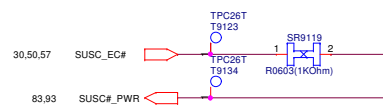
SUSC#_PWR POWER



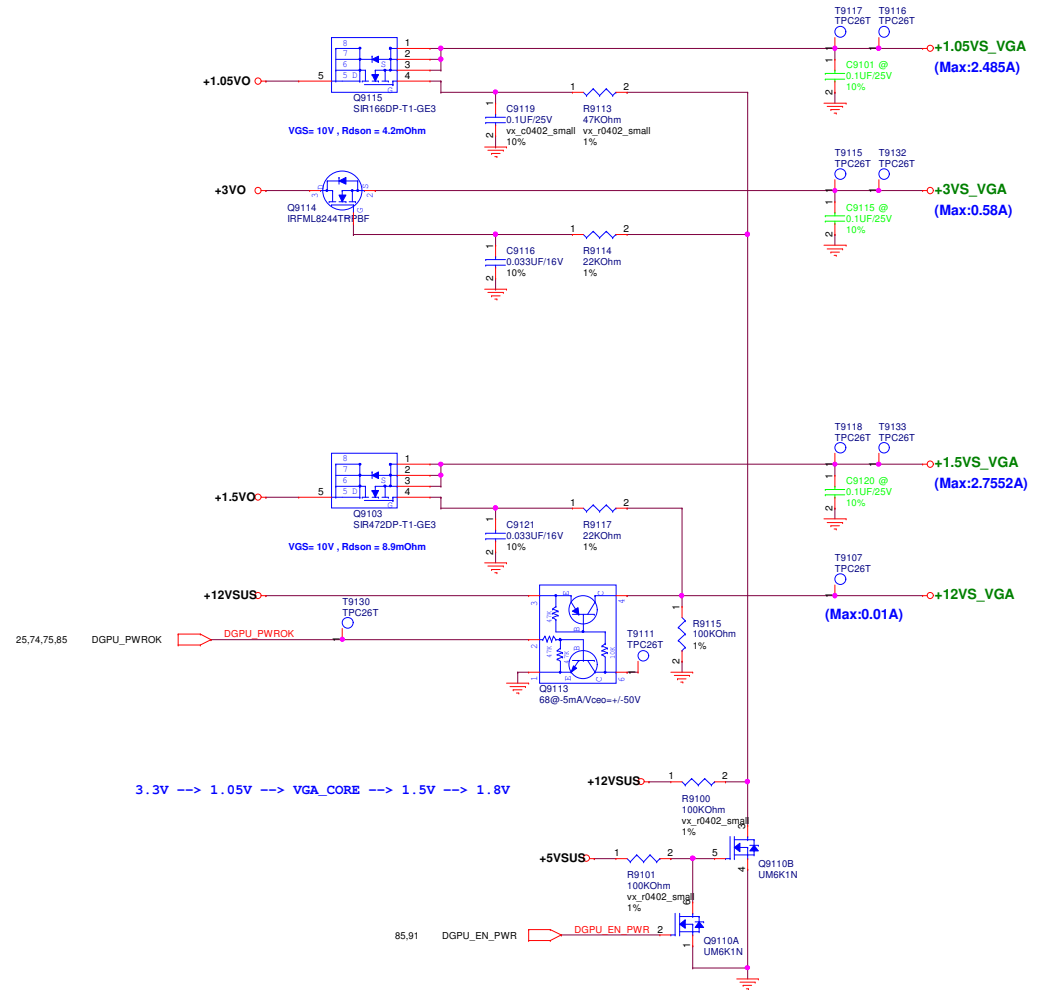
SUSB#_PWR POWER Control



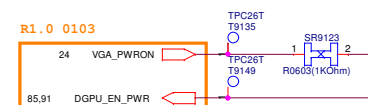
SUSC#_PWR POWER Control



DSC#_PWR POWER(dGPU)

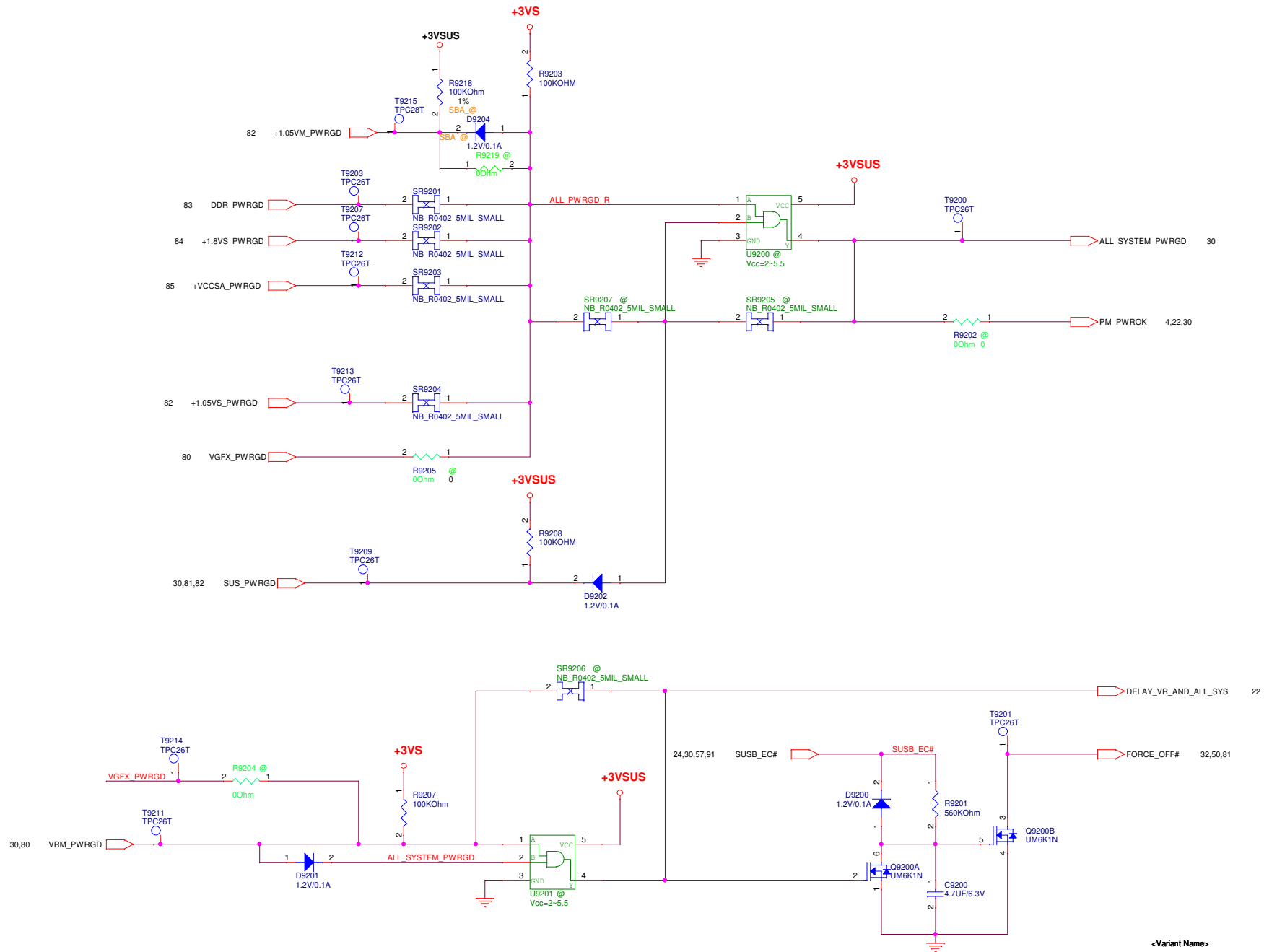


DSC_VGA_PWR POWER Control



<Variant Name>		Title : POWER_LOAD SWITCH	
PEGATRON		Engineer: Clark Liang	
Size	Project Name	U14	Rev
Custom			1.0
Date: Wednesday, February 01, 2012	Sheet	91	of 94

POWER GOOD DETECTOR



<Variant Name>

AC_BAT_SYS AC_BAT_SYS 45,81,88
BAT BAT 88
BAT_CON BAT_CON 60,88

BAT1_CON BAT1_CON 60
BAT2_CON BAT2_CON 60

+3VA +3VA 6,20,27,30,56,57,81,88
+5VA +5VA 50,52,56,81
+5VO +5VO 80,81,82,83,85,91
+3VO +3VO 81,84,85,91
+1.05VO +1.05VO 82,91
+0.75VO +0.75VO 83
+1.5VO +1.5VO 83,91
+1.8VO +1.8VO 84

+5VSUS +5VSUS 27,52,81,91
+3VSUS +3VSUS 22,24,27,28,30,33,53,56,81,92
+12VSUS +12VSUS 81,91

+5V +5V 52,55,56,57,66,91
+3V +3V 24,40,53,55,57,62,91
+12V +12V 91

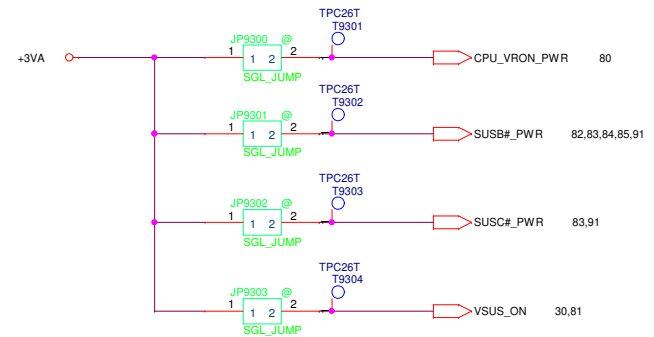
+5VS +5VS 27,30,31,38,46,48,50,51,53,56,57,80,91
+3VS +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+12VS +12VS 20,28,48,91
+1.05VS +1.05VS 26,27,82,85
+0.75VS +0.75VS 16,17,57,83
+1.5VS +1.5VS 26,53,57,91
+1.8VS +1.8VS 7,25,26,80,84
+VCCSA +VCCSA 7,85

+VCORE +VCORE 6,9,11,80
+VGFX_CORE +VGFX_CORE 7,9,80

+12VS_VGA +12VS_VGA 91

+1.5VS_VGA +1.5VS_VGA 57,91
+1.05VS_VGA +1.05VS_VGA 57,91
+3VS_VGA +3VS_VGA 57,75,91

FOR POWER TEST



<Variant Name>

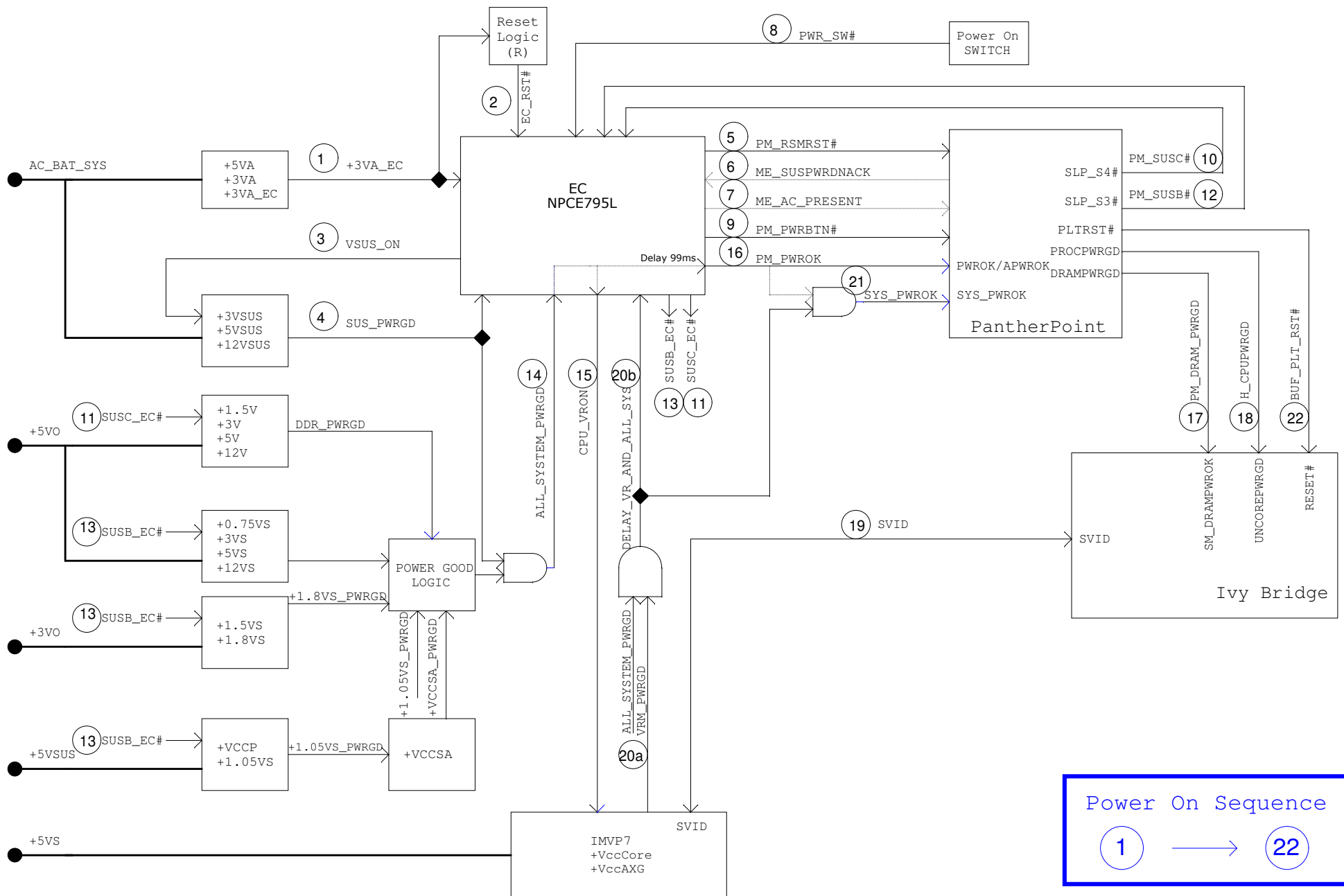
PEGATRON		Title :POWER SIGNAL	
		Engineer: Clark Liang	
Size	Project Name		Rev
Custom	U14		1.0
Date: Wednesday, February 01, 2012		Sheet	93 of 94

modify notice R11 to R12

Version	Date	Description
20120103		change SP604 to SP0605, SP605 to SP0606, JP3805 to SP3805, R2240 to SR2201 change SP5501,SP5502 to small size change SP2703~SP2708, SP2715 to small size Add R2208~R2212 P60 Add daul battery schematic P48 modify HPD schematic P22 modify SYS_PWRGD schematic change J4001,J4002 part change PCIE and SATA and USB2.0 and USB3.0 C
20120105		change SP4001,SP4601,SP4602 to small size change SP2003,SP2005,SP2110,SP2114~SP2116,SP2209,SP2210,SP2212~SP2215 to small size change SP2304,SP2305,SP2401,SP2402,SP2501,SP2502,SP3002,SP3006 to small size change R5103 to 0805 modify P53 schematic
20120109		add R4810~R4813 remove SP3101~SP3124
20120110		add C0794
20120111		add CN3101~CN3106
20120112		add project ID R2530, R2533 add D5601,D5602,R2713,R2714
20120113		add wifi LED R5609,R5616,R5617,T2517

PEGATRON		Title : SYSTEM History	
<OrgName>		Engineer: Trunks_Chen	
Size Custom	Project Name B34		Rev 1.0
Date: Wednesday, February 01, 2012		Sheet 95 of 99	

Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]



Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]

